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Variable-Order Ant System for VLSI multiobjective floorplanning

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ABSTRACT

Floorplanning is crucial in VLSI chip design as it determines the time-to-market and the quality of the product. In this work, Variable-Order Ant System (VOAS) is developed and combined with a floorplan model namely Corner List (CL) to optimize the area and wirelength. CL is used to represent the floorplan layout. Although CL has proven to have the same search space and time complexity as Corner Sequence (CS), comparatively, CL has more corners to be selected. This compensates the sequence weakness, where modules can be placed freely onto the corners, which are not bounded by the floorplan contour. Two groups of ants, namely VOAS and reconnaissance ants, which will collaborate with each other to determine the local information, are introduced. Through this cooperation, VOAS ant can ascertain its local information greedily, based on the local search space information carried out by reconnaissance ants. Subsequently, VOAS ant proposes a new variable-order property to prioritize the global and local explorations. The variable-order property enables the ants in VOAS to weigh a better choice of modules for the floorplanning, based on the local and global information. The update rules of VOAS are modified in order to handle two-dimensional problem, such as VLSI floorplanning. VOAS shows improved results in terms of purely area optimization as well as composite function of area and wirelength, as compared to other state-of-the-art and recent floorplanning/placement algorithms based on Microelectronics Centre of North Carolina (MCNC) and Gigascale Systems Research Center (GSRC) benchmarks.

1. Introduction

In modern integrated circuit (IC) design, a floorplan of an IC is a schematic representation of its major functional blocks. As technology advances, the number of transistors in a very-large-scale integration (VLSI) design has increased rapidly obeying Moore's law [1] whereas the features of IC have progressively scaled down. Moore's law states the number of transistors in a chip doubles in approximately every two years. This encourages the extension of the chip's functions while maintaining the size of the chip. Hence, the circuit density and VLSI design complexity of an IC have increased rapidly. As the features of the VLSI chip shrinks over-time, many factors such as the total wire length, time delay, routing congestion and overall power consumption, will affect the reliability and performance of the chip. To regulate these issues, efficient floorplanning is required as it dictates the quality of the VLSI design. VLSI floorplanning design is a well-known Non-deterministic Polynomial-time hard (NP-hard) problem [2,3] and thus, it is difficult to find ideal optimal solutions in practical applications. However, near-optimal solutions are attainable with the aid of combinatorial optimization.

Floorplan layouts are modeled in a graph-based [3–9], tree-based [10–13] or sequence-based representation [14–16] and optimized using tools such as mathematical programming [17] or artificial intelligence (AI) technique [16,18,19]. Although there are a number of metaheuristic algorithms adapted in VLSI floorplanners such as Genetic Algorithm (GA) [20], and Evolutionary Algorithm (EA) [16] and many more, Simulated Annealing (SA) [21] is preferred due to its easiness and flexibility to be adapted in different type of floorplan models. However, fairly huge computational resources are required in SA due to its semi-exhaustive nature [22] and thus unable to handle large scale VLSI floorplanning problems [23]. In Hierarchical Congregated Ant System (H-CAS) [19], SA optimization results are validated to be only marginally better than random-based searching algorithm's as the number of modules in the VLSI floorplanning problem increases. This is due to the high dependency of SA approach on the initial solution generated and the size of the problem. SA tends to be trapped into local optima when the scale of the problems increases.

Swarm intelligence is a relatively new metaheuristics approach inspired by the sociable nature behaviors of insects or animals. Subsequently, ants have inspired a number of techniques in optimizing the problem solving. After the first ant-based metaheuristics, namely Ant System (AS) [24] was developed, AS was further improved in [25] and was called as Ant Colony System (ACS) algorithm. As a promising and fruitful metaheuristics, ant-based metaheuristic algorithms have been successfully

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adapted in many types of NP-hard problems such as Traveling Salesman Problem (TSP) [26], asymmetric TSP [27], minimum weight vertex cover problem [28], and structural topology optimization [29].

1.1. Our contributions

In this paper, a new metaheuristic algorithm namely Variable-Order Ant System (VOAS) is proposed to handle VLSI standard cells floorplanning with optimized utilization of chip area or composition of both chip area utilization and wirelength. As a start of, a sequence-based representation called Corner List (CL) is developed to model the floorplan layouts where the transformation between the representation and the layouts can be carried out in a linear runtime. CL characteristics such as computational complexity and search space are compared to the existing sequence-based state-of-the-art representations, namely Corner Sequence (CS) [14] and Moving Block Sequence (MBS) [15,16]. With a larger search space, CL can perform the transformation between floorplan layout and representation n times faster, as compared to MBS. Even though the search space and time complexity of CL are same as CS, CL introduces more corners than CS as the latter only considers the corners bounded by the floorplan contour. Thus, CL can search more corners than CS within same period of time. Since contour is generated by previously placed modules, CL allows compensation of sequence weakness, where modules can be placed freely onto any corners, including those which are unbounded by the contour. This CL modeling is very important as it enables ant-based metaheuristics to search for near-optimal solution in a large search space.

Inheriting the major properties of Ant System (AS), VOAS has adapted a unique variable-order property in route selection mechanism and modified the pheromone update rule, in order to handle VLSI floorplanning. This variable-order property of VOAS utilizes the inter-dependency of the local and global information in order to ensure the later modules selected in the sequence list will always be greedily placed onto the floorplan. High dependency on global information at the beginning of the module floorplanning is crucial as the ants in the floorplanning can make a better decision based on the previous experience. This property allows a perturbation which might lead to a better near-optimal solution. The importance of the global information will decrease gradually as the floorplanning approaches the final stage. Emphasizing on the local information during the finalization of the floorplanning, greedy VOAS ant completes the floorplanning by choosing the remaining corner with less whitespace/wirelength. A wrong choice by the ant in area-based problem will result in an unacceptable huge whitespace being created especially approaching the end of the process, as shown in Fig. 1. Similarly, an improper choice in wirelength-based VLSI floorplanning problem will lead to a floorplan layout with higher wirelength. This interchangeable priority of VOAS not only enables the ant to search for possible near-optimal solutions but also completes the floorplanning effectively. Analogically, the global information is represented by the pheromone while the instant local information is found through the cooperation between the VOAS ant and reconnaissance ants (RAs) where RAs search for the instant local search information greedily. An experiment is carried out to compare the efficiency of VOAS with commonly used ant-based metaheuristics, namely AS. VOAS shows improved results in terms of area and wirelength optimization.

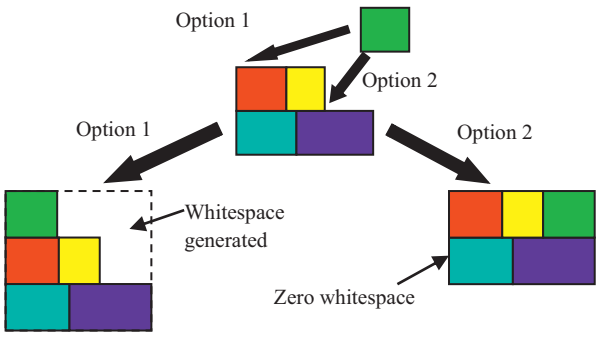

Fig. 1. Whitespaces created for different final module selection by ant.

This article is organized as follows: Section 2 reviews the newly developed CL representation where the properties of the CL are proven mathematically. Section 3 discusses the characteristics of AS algorithm. Section 4 highlights the proposed VOAS algorithm and how VOAS handles VLSI floorplanning problem. In Section 5, the experimental results are compared with the state-of-the-art and recent floorplanning algorithms. Finally, the conclusion is drawn in Section 6.

2. Floorplan layout modeling

In this section, a new floorplan representation is presented, namely corner list (CL). For the ease of understanding, the technical notations used in CL are defined below:

Definition 1. Two dummy modules m_{bottom} and m_{left} are assumed to be located at bottom and left boundaries of the floorplan, with the dimensions of (width, height) equal to $(\infty, 0]$ and $[0, \infty)$ respectively.

Definition 2. Given a set of selected modules $S \subset M$, and arbitrary corner in the set of corner list C, namely $[C_{left}, C_{bottom}]$, then $C = \{C_{left}, C_{bottom}\} \subset (S \cup \{m_{left}, m_{bottom}\})$.

Definition 3. For arbitrary corner $[C_{left}, C_{bottom}]$ with corner modules C_{left} and C_{bottom}, assume the coordinates of the top-right corners of C_{left} and C_{bottom} are denoted as $(x_{TR\text{-}left}, y_{TR\text{-}left})$ and $(x_{TR\text{-}bottom}, y_{TR\text{-}bottom})$ respectively, then, the corner is realizable under the conditions of $x_{TR\text{-}bottom} \geq x_{TR\text{-}left}$ and $y_{TR\text{-}left} \geq y_{TR\text{-}bottom}$.

Definition 4. CL consists of two tuples where the first tuple represents the sequence of modules chosen and the second tuple denotes the sequence of the corners chosen by the corresponding modules. CL can be represented as:

$$\mathrm{CL} = (\Omega, \chi)$$

where

$$\Omega = (\Omega_1, \Omega_2, \ldots, \Omega_n); \quad \Omega_i = m_i \in M, \quad \Omega_i \neq \Omega_j, \quad 0 \leq i, j \leq n,$$

$$\chi = (\chi_1, \chi_2, \ldots, \chi_n); \quad 0 \leq i, j \leq n,$$

$$\chi_i = \begin{cases} [m_{left}, m_{bottom}]; & i = 1 \\ [C_{left-i}, C_{bottom-i}]; & 2 \leq i \leq n \end{cases}$$

2.1. CL matrix representation

In the CL representation, modules are placed one at a time according to a predefined sequence. After numerous permutations of modules placement, a CL matrix is formed. Let us consider an $(n \times 3)$ CL matrix, shown in matrix (1), where n is the number of modules placed in the layout. There are 3 configurations concluding the placement of a particular module. The first column represents the first tuple which is the sequence of modules to be