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Distributed Monitoring System For Reconfigurable Computer Systems*

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Abstract

The paper covers the history of development of reconfigurable computer systems including currently being developed modern system with independent circulation of the cooling liquid. The authors introduced the distributed monitoring system for reconfigurable computer systems which provides continuous status diagnostics of the computational module components for reduction of the low-productive time periods of equipment and for minimization of burden when worst-case situations are detected. High cooling efficiency with power reserve for the designed perspective FPGA families, resistance to leaks and their consequences, and compatibility with traditional water cooling systems based on industrial chillers are the distinctive features of the designed immersion liquid cooling system.

Keywords: FPGA, reconfigurable computer systems, liquid cooling system, hardware monitoring system

1 Introduction

One of perspective approaches to achieve high real performance of a computer system is adaptation of its architecture to a structure of a solving task, and creation of a special-purpose computer device which hardwarily implements all computational operation of the information graph of the task with the minimum delays. A natural requirement for a modern computer system is hardware support of modification of both the algorithm of the solving task and the task itself, that is why FPGAs are used as a principal computational resource of reconfigurable computer systems [5].

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The main advantages of programmable logic devices (PLD) are possibility of implementation of complicated parallel algorithms, availability of CAD-tools for complete system simulation, possibility of programming or modification of in-system configuration, compatibility of various design projects when they are converted in a VHDL, AHDL, Verilog descriptions or in any other hardware description language.

The history of the PLD architectures started in the end of the 1970s, when the first PLDs with programmable-AND and programmable-OR arrays appeared. Such architectures were called FPLAs (Field Programmable Logic Array) and FPLSs (Field Programmable Logic Sequencers) [6]. Their main disadvantage is weak use of programmable-OR array. Introduction of FPGAs (Field Programmable Gate Array) ignited revolution of devices with programmable logic. The FPGA class includes Xilinx XC2000, XC3000, XC4000 and Spartan, Actel ACT1, ACT2, Altera FLEX8000 family and some Atmel and Vantis PLDs.

The FPGA configurable logic blocks (CLBs) are connected by a programmable switch matrix. The logic blocks consist of one or several rather simple logic cells based on a 4-input look-up table (LUT), a program-controlled multiplexer, a D-flip-flop. Input/output blocks (IOB) that provide bidirectional input/output, tri-state, etc., are typical for the FPGA-architectures. The FPGA chips have the following advanced features: a JTAG port that supports all mandatory boundary-scan instructions specified according to the IEEE 1149.1 standard and a master configuration mode (that required a build-in oscillator).

The FPGAs with a dedicated block RAM were the result of further development of the FPGA architecture, owing to which the FPGAs can be used with no external memory devices. The FPGAs have a high logic capacity, an easy-to-use architecture, a quite high reliability and an optimal ratio "price/logic capacity", therefore they match various requirements, claimed by circuit engineers.

In 1998-1999 augmentation of FPGA equivalent logic capacity had changed attitude to CAD-tools of both software developers and users. Till the end of the 1990s the main tool of project description and schematic entry was a graphic editor and libraries of standard primitives and macros such as logic elements, elementary combinational and sequential functional units, analogues of standard integrated circuits of small-scale and medium-scale integration. At present, circuit engineers widely use hardware description languages for FPGA-based implementation of algorithms. Besides, up-to-date CAD-tools support both standard hardware description languages (such as VHDL, Verilog) and specialized hardware description languages developed by FPGA vendors specially for their own needs, CAD-tools and FPGA families with special architecture features. Such example is AHDL (Altera Hardware Description Language), which is supported by the Altera CAD-tools MAX PLUS II and Quartus. HDL-languages are very user-friendly tools for description of various interfaces, but implementing complicated calculations the developer cannot influence the mapping of HDL code on hardware resource of the chip and this has some negative influence on efficiency of the implementation. Besides, it is obvious that circuit description is evident, so when we implement some complex computational algorithm we prefer use a graphic editor.

FPGAs, as any other complex systems, need specialized tools for monitoring of their condition. Since the 5th family all Xilinx FPGAs contain specialized monitoring units called a System Monitor [13]. With the help of a JTAG-interface, it is possible to receive various information from the system monitor concerning FPGA condition. Such information contains temperature, power supply voltage, warning that the temperature critical value is achieved in the FPGA core. Information, received from the system monitor, together with information, received from other devices of a computational module, is the principal source of data in the designed distributed monitoring system for reconfigurable computer systems.