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A Perspective on Collaboration with Interconnects & Routing in Network on Chip Architectures

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Abstract

As VLSI technology advances, the number of modules on a chip multiplies and thus the solutions for on-chip communication are evolving to support the new paradigm in inter-module communication on System on Chip (SOC). Those System on Chip, Current chip designs incorporate more complex multilayered and stack segmented interconnection buses with various routing architectures results in a Network on Chip. These, traditional solutions, which were based on a combination of shared-buses and dedicated module-to-module wires, scalability limit, and are no longer adequate for System on Chip/Network on Chip. On-chip architectures have been optimized for a non-chip environment before the multi-core challenge became the focus of processor chip architecture through the latency and the throughput. This evolution of on-chip interconnects may evoke feelings of among networking old-timers. The considerations that have driven data communication from shared buses to packet-switching networks and to routing protocols such as spatial reuse, multi-hop routing, flow and congestion control etc., will inevitably drive the challenges raised in the design of network interfaces with the segmented stack layered mechanism, and potentially managing the critical resources designed for on-chip modules.

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1. Introduction

Currently, the chip design is to incorporate a full-fledged network-on-a-chip (NOC) consisting of a collection of links and routers and a new set of routing protocols that govern their operation. The survey reasons for the inevitable shift to NOCs in the VLSI world, while exposing the most important requirements from the NOC[1]. The aim is to expose the networking with system to the concept of network-on-chip (NOC) as a realm, within the VLSI in which the networking among the multi-cores plays a significant role in exploring the solutions such as network design, routing, and quality-of-service (QoS), unfamiliar settings under new constraints of VLSI. In order to stimulate some specific research directions, arising in each of these categories, focus is made on routing and resource allocations for the cores.

The first step was to address the low level challenges in designing on-chip interconnects in presence of deep sub-micron technologies. Due to the increased role of noise sources such as crosstalk, power-supply noise,

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soft errors, etc. physical link design will not suffice to provide communication reliability, and the proper course of error-control actions will have to be taken at higher levels of abstraction[2].

As a second step, the system level NOC design came up with an on-chip architecture, which can be used to instantiate application-specific MPSOCs consists of network building blocks/cores that can be arbitrarily tuned and composed at instantiation time on the network stack layer, and investigating how communication reliability can be traded-off with power, aware that the implementation of delays between the modules taken place[3]. This solution provides the flexibility at the cost and also size for an increased design complexity by placing in stacks. Two relevant features are the use of deeply pipelined switches and of link pipelining, which decouples link throughput from the worst case link delay in the design. Therefore, the operating frequencies in the order of multi-GHz range can be achieved. Xpipes is one of the most advanced NOC designs targeting heterogeneous MPSOCs with customized domain-specific communication architectures[4,5].

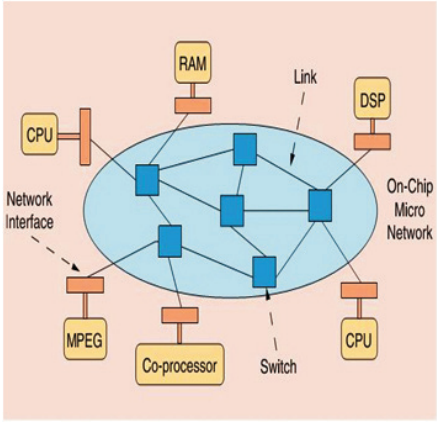

Fig. 1. An example for NOC Architecture.

2. Routing in NOC

A router must perform two fundamental tasks: **Routing** and **Packet forwarding**. The NOC is a system of communication between the core entities segmenting into smaller modules, such that the difference between the NOC and SOC for the system, is illustrated as SOC is a single layer application centered logic device and the NOC as the multiple layered of stacks placing the applications driven on a SOC mounting with each layer so as to minimize the effectiveness of area, delay between the core applications, The NOC interconnects in different stacks, where different layers implement on different cores in the blocks of the interconnect. The power of traditional protocol stacks, such as TCP-over-IP-over-Ethernet, is such example that the information at each layer is encapsulated by the layer below it. The routing of the NOC implementation comes from the same core source and the encapsulation of such information at each layer for the protocol stack is routed with interconnects for the layers of the core data. The routing & interconnections of such modules on a generic SOC is shown in Fig. 2 below.

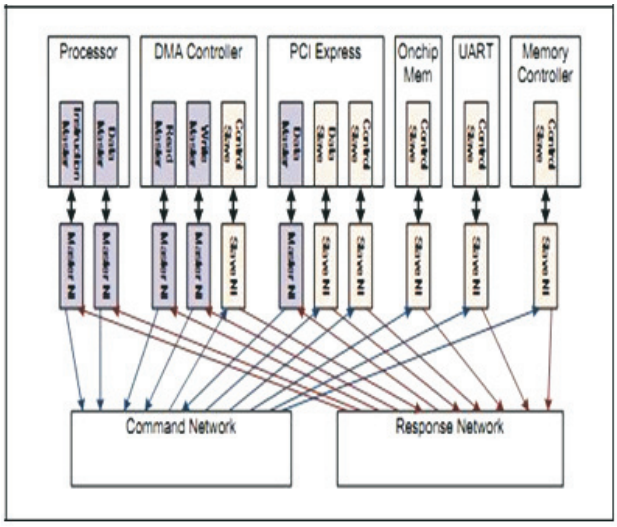

Fig. 2. Routing to Blocks in Generic SOC.

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