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Soft processors as a prospective platform of the future

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Abstract

Modern field-programmable gate arrays (FPGA) play a very important role in designing of new soft CPUs and integrated systems-on-chips. Compared to an application-specific integrated circuit (ASIC), FPGAs provide the highest degree of flexibility being almost fully application neutral. The price of such flexibility is higher usage of basic logic gates and decrease in circuit operating frequency caused by the use of switched interconnect fabric as opposed to fixed metal interconnect defined by masks at manufacturing for ASIC.

However due to more regular and less complex FPGA structure they lead in terms of new IC manufacturing technologies adoption. Therefore we can expect next generation of general purpose FPGA devices based on 14 nm norms in 2017.

This article examines the applicability of Moore's Law to general purpose FPGAs, using datum for Xilinx Spartan and Altera Cyclone families. On the basis of the obtained data the conclusion that in the near future FPGAs become a prospective platform for general purpose CPUs implementation is drawn.

Keywords: Moore's law, soft CPU, FPGA, Spartan, Xilinx, Cyclone, Altera, OpenRISC

1 Introduction

Soft CPU is a microprocessor kernel implemented on an FPGA device using methods of logical synthesis from standard logic elements (LE), arithmetic units (AU) and distributed memory cells.

There is always an engineering choice between general purpose and application specific digital devices.

FPGA device, compared to an ASIC, provides the highest degree of flexibility being almost fully application neutral. The price of such flexibility though is higher usage of basic logic gates (transistors) and decrease in maximum circuit operating frequency caused by the use of switched interconnect fabric as opposed to fixed metal interconnect defined by masks at manufacturing for ASIC.

But if we look at the history of computing, modern ASIC CPUs are less efficient compared to special purpose CPUs, still widely used for time critical or special applications. Nevertheless

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the reduction in difficulty of device implementing such functions justifies the use of general purpose CPUs (MPUs). Similarly the use of FPGA-based soft-CPUs allows speeding up the development of such device features that can be primarily implemented only in hardware – security, special functions, time critical and deterministic functions that require exact and predictable timing.

In contrast to ASIC solutions soft-CPUs allow:

- improve or fully replace CPU architecture and eliminate defects in the field;
- implement hard logic solutions with maximum reliability and information security;
- implement functions that can be efficiently implemented only with hard logic, for instance coding/decoding and hashing algorithms;
- implement functions that require hard deterministic and fixed timing.

In particular – hardware interfaces protocols implementation:

- significantly reduce components nomenclature by avoiding interface ASICs;
- standardize hardware component of digital control system for different products;
- avoid undocumented "black box" components in the design (full control over technologies used).

2 Applicability of Moore's law for general purpose FPGA devices

2.1 Main metrics

Main metrics used to compare ASIC and FPGA-based soft-CPUs implementations that determine their performance are the number of gates (transistors) and maximum internal clock frequency. Modern FPGAs also include distributed memory blocks and embedded blocks – such as ALU, DSP and communication protocol engines.

Elementary switch is single of multiple gate FET or complimentary pair, whereas LE corresponds to low-level integration IC, and consists of 20..30 elementary gates. Static memory cell consists of 3..6 gates.

We use the following equation to estimate the equivalent gates counts for ASIC corresponding to FPGA metrics:

$$N_{eq} \approx 2 \times N_{LE} + 4 \times N_{bit} \tag{1}$$

N_{LE} – number of FPGA logic elements.

N_{bit} – number of FPGA distributed RAM bits.

Maximum clock freq for FPGA based soft-CPU is usually 3..5 times lower then for ASIC implementation, since in FPGA clock signal must pass through several statically controlled FET switches with resistance considerably higher then of ASIC's metal interconnect.

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