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Linearization of High Power Amplifier Using Modified Artificial Bee Colony and Particle Swarm Optimization Algorithm

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Abstract

A linearization method for power amplifiers is proposed to cancel out distortion induced during amplification. Wiener model is chosen for power amplifier modelling. The linearization is achieved by the Modified Artificial Bee Colony (ABC) and Particle Swarm Optimization (PSO) algorithm. The Modified ABC and PSO algorithm reduces the complexity in linearization. Experimental results obtained for the proposed method shows that a better linearization of the amplifier characteristics can be obtained using the proposed method.

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Keywords: Optimization, Artificial Bee Colony algorithm, Particle Swarm Optimization, Wiener model

1. Introduction

Power amplifiers are unavoidable components in every transmission systems and are nonlinear in nature. The nonlinearity leads to widening of signal bandwidth above the allotted limits, which leads the transmission to interfere with nearby channels. It also causes distortions within the signal bandwidth, which reduces the bit error rate at the receiver. Newer modulation formats, such as WCDMA or OFDM, are especially vulnerable to the nonlinear distortions due to their high peak-to-average power ratios (PAPRs). We can simply back-off the input signal to achieve the linearity required for the power amplifier, but this result in low power amplifier efficiency. Alternatively we can linearize a nonlinear power amplifier so that overall we have a linear and reasonably efficient

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transmission system. Digital pre-distortion (DPD) is one of the most cost effective ways [1] among all linearization techniques. However, most of the existing designs treat the power amplifier as a memoryless device. For wideband or high power applications, the power amplifier exhibits memory effects, for which memoryless pre-distorters can achieve only limited linearization performance.

The DPD scheme adds a digital pre-distorter in the baseband to create an expanding nonlinearity that is complementary to the compressing characteristic of the power amplifier. The combination of the pre-distorter and the power amplifier becomes linear and the original input is amplified by a constant gain [2]. With the pre-distorter, the power amplifier can be utilized up to its saturation point while still maintaining a good linearity, thereby significantly increasing its efficiency. In reality, the power amplifier characteristics may change over time because of temperature drift, component aging, *etc*. Therefore, the pre-distorter should also have the ability to adapt to these changes.

Digital pre-distortion implementations mostly focus on the power amplifier that has a memoryless nonlinearity; i.e., the current output depends only on the current input through a nonlinear mechanism. This instantaneous nonlinearity is usually characterized by the AM/AM and AM/PM responses of the power amplifier, where the output signal amplitude and phase deviation of the power amplifier output are given as functions of the amplitude of its current input. As the signal bandwidth gets wider, such as in WCDMA, power amplifiers begin to exhibit memory effects. This is especially true for those high power amplifiers used in wireless base stations. The causes of the memory effects can be attributed to thermal constants of the active devices or components in the biasing network that have frequency dependent behaviors. As a result, the current output of the power amplifier depends not only on the current input, but also on past input values. In other words, the power amplifier becomes a nonlinear system with memory. For such a power amplifier, memoryless pre-distortion can achieve only very limited linearization performance. Therefore, digital pre-distorters also need to have memory structures.

2. Literature survey

Sheng Chen [1] has suggested that digital pre-distorter remedy is alluring on account of its minimal on-line computational complexity, insignificant memory-units needed and the easy VLSI hardware configuration execution. In addition, the devised pre-distorter is competent to efficiently recompense the grave nonlinear distortions and memory impacts triggered by the memory HPA functioning in the output saturation horizon. The replication outcomes achieved are listed out to authenticate the efficacy of the innovative pre-distorter design.

Biyi Lin, Yide Wang, Bruno Feuvrie and Qingyun Dai et al [2]. Power amplifier linearization techniques are very important to reduce the distortion of the transmitted signal and the adjacent band interference of users. As its facility of implementation, adaptive ability and high efficiency, the pre-distortion technology becomes the first choice to minimize the nonlinear distortions. A new technique, based on the pre-distortion principle for linearizing a power amplifier, which is modeled by a Wiener model, is proposed. The Wiener model is used to take into account the nonlinearities and the memory effects of the power amplifier. Also propose an efficient and original method for extracting the parameters of the power amplifier's Wiener Model. Simulation results have been provided for showing the performances of this technique.

Bipin P.R and P.V Rao [3]has compared the use of ABC and PSO algorithms for the purpose of linearization of power amplifiers. From the experimental results they have found that the PSO algorithm provides good results compared to ABC algorithm.

Landin *et al*. [4] proficiently launched a direct model structure for defining the class-D out phasing power amplifiers (PAs) and a novel method for digitally pre-deforming these amplifiers. The direct model configuration was dependent on the modeling divergences in gain and delay, nonlinear interfaces between the two paths and divergences in the amplifier attitude. The digital pre-deformation technique was devoted to function only on the phases of input signal, duly rectified for both amplitude and phase mismatches. This eventually dispensed with the requirement for the supplementary voltage supplies to recompense for the gain mismatch. The Model and pre-deformation functioning were effectively evaluated on a 32 dBm peak output power, class-D out phasing PA in CMOS with on-chip transformers.