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Implementation of Digital Modulator Using Digital Multiplier for Wireless Applications in Verilog and Cadence

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Abstract

The digital communication is more advantageous than analog communication. Digital components and subsystems are easy to build than analog components. As the implementation in VLSI technology progressed, the cost of the integrated circuits is gradually reduced. The components used in digital communication systems are robust and insensitive to atmospheric conditions and ensures good protection against noise and interference.The digital design offers more flexibility than analog design. The proposed digital Quadrature Phase Shift Keying(QPSK)modulator is based on digital multiplier called booth multiplier. This work is simulatedin Integrated Simulated Environment (ISE), Incisive simulators of Xilinx9.1i and Cadence tool respectively. The code is synthesized using Cadence RTL compiler and implemented on Field Programmable Gate Array (FPGA) spatan3 kit.The performance parameters such as power, area, and timing are analyzed and compared. This proposal gives better results than the conventional method of using analog multiplier for QPSK system.

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1. Introduction

One of the basic problems of communication engineering is the design and analysis of systems.This allows many individual messages to be transmitted simultaneously over a single communication channel.The technique used for multiple transmissions is called multiplexing. The multiple access techniques are Frequency Division Multiple Access (FDMA), Time Division Multiple Access (TDMA) and Code Division Multiple Access (CDMA).The advanced modulation techniques are used with multiple access technology to increase the data rate of a communication system,on the same available spectrum [1]. The higher order modulation techniques are more bandwidth efficient than

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lower order modulation techniques. Comparing QPSK (Quadrature Phase Shift Keying) modulation system with the BPSK (Binary Phase Shift Keying), QPSK is more bandwidth efficient than the BPSK. In this paper, QPSK modulation system implementation is shown using 8-bit Booth Multiplier. Since the parameters of the analog multiplier, various with the changes in the atmospheric conditions. The analog multiplier is replaced by digital multiplier. The first part of the paper explains about the basic digital communication block diagram and description [2, 3]. The second part of this paper describes the conventional method of QPSK system. The third part discriminate the Booth Multiplier for QPSK system. The fourthpart distinguishes and trace out the results, analysis and comparison.

1.1. Introduction to Digital Communication System

The communication can be analog or digital. It may be wire-line or wireless.The telephone, television, radio, FAX and e-mail are the various forms of communication.These are all become an integral part of our daily lives. Life cannot be imagined without them.

The basic digital communication block diagram is shown in Fig1. It consists of the source, the source encoder, channel encoder and digital modulator at the transmitter side. The digital demodulator, the channel decoder and source decoder at the receiver side. The physical channel connects the transmitter and the receiver.

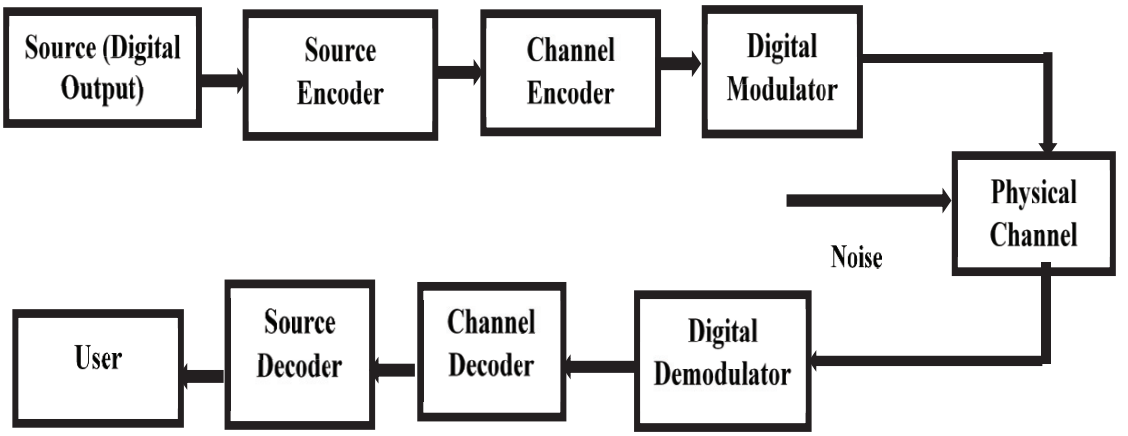

Fig. 1. Basic digital communication block diagram.

- The original information signal is converted in to digital format by using analog to digital converter.
- Source encoder does the data compression by avoiding redundancy in the incoming bit stream.
- Channel encoder introduces redundancy into the bit stream at its input in order to provide some amount of error-correction capability to the data being transmitted.
- Digital modulator and demodulator are used for mapping and de-mapping the data respectively.
- Finally channel and source decoders reproduces the data.

1.2. Conventional Quadrature Phase Shift Keying (QPSK) System

The Quadrature Phase Shift Keying (QPSK) is one type phase of modulation system. The phase angle of the carrier signal is varied according to the message signal. The conventional QPSK system consists of analog multiplier is shown below in Fig. 2.The QPSK signal is represented as shown in the equation (1). The four possible phase signals of QPSK are $\Pi/4$, $3\Pi/4$, $5\Pi/4$ and $7\Pi/4$. In equation (1) the E is the signal energy and τ is the symbol duration. The four phases can be represented in gray encoded dibits as 11, 01, 00 and 10 respectively. The QPSK gives the same bit error rate as that of the BPSK, but requires only half the bandwidth required for BPSK. Since the symbol duration for QPSK is