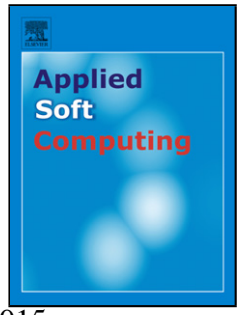
Accepted Manuscript



Title: FPGA based hardware implementation of Bat Algorithm

Authors: Mohamed Sadok Ben Ameur, Anis Sakly

PII: S1568-4946(17)30187-4
DOI: http://dx.doi.org/doi:10.1016/j.asoc.2017.04.015
Reference: ASOC 4148

To appear in: *Applied Soft Computing*

Received date: 4-5-2016
Revised date: 8-3-2017
Accepted date: 10-4-2017

Please cite this article as: Mohamed Sadok Ben Ameur, Anis Sakly, FPGA based hardware implementation of Bat Algorithm, Applied Soft Computing Journalhttp://dx.doi.org/10.1016/j.asoc.2017.04.015

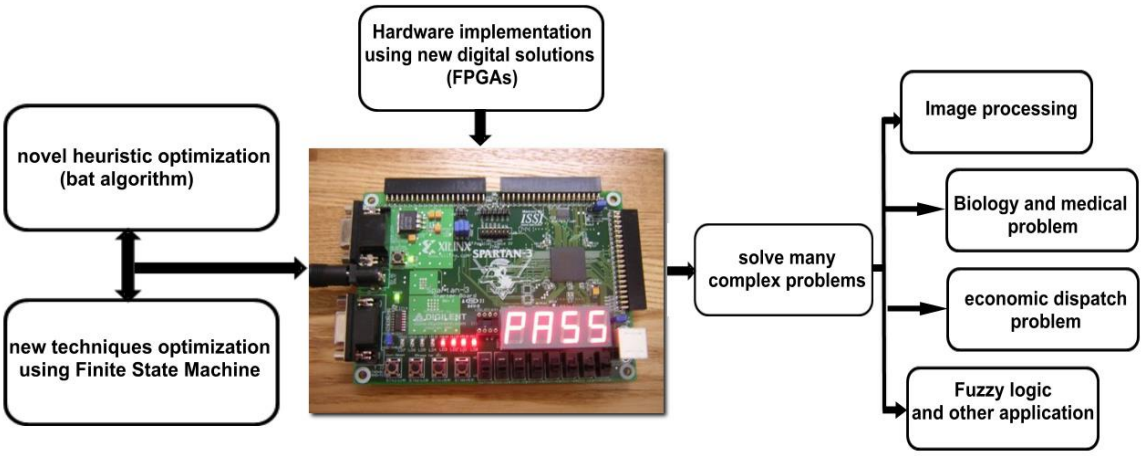
This is a PDF file of an unedited manuscript that has been accepted for publication. As a service to our customers we are providing this early version of the manuscript. The manuscript will undergo copyediting, typesetting, and review of the resulting proof before it is published in its final form. Please note that during the production process errors may be discovered which could affect the content, and all legal disclaimers that apply to the journal pertain.

ACCEPTED MANUSCRIPT

FPGA based hardware implementation of Bat Algorithm

Mohamed Sadok BEN AMEUR[1,2], Anis SAKLY[2],
[1:] Laboratory of Electronic and Microelectronic, University of Monastir, Tunisia.
Mohamed sadok ben ameur, msba2014@gmail.com
[2:] Research unit ESIER, National Engineering School of Monastir, University of Monastir, Tunisia.
Anis sakly, Sakly_anis@yahoo.fr,

Graphical abstract



Download English Version:

https://daneshyari.com/en/article/4963181

Download Persian Version:

https://daneshyari.com/article/4963181

Daneshyari.com