A Compensation Band-limited Digital Predistortion for Wideband Power Amplifiers

Bo Yang
Space Star Technology Co., Ltd.
Beijing, China
bagoiyb_rai@126.com

Linhai Gu
Space Star Technology Co., Ltd.
Beijing, China
215718571@qq.com

Jiangchun Liu
Space Star Technology Co., Ltd.
Beijing, China
jiangchun_liu@163.com

***Abstract*—This paper presents an efficient compensation band limited digital predistortion (CBL-DPD) architecture for the wideband Orthogonal Frequency Division Multiplexing (OFDM) transmitter system. Compared with traditional band limited digital predistortion (BL-DPD), the CBL-DPD adds a low pass filter (LPF) and an error compensation term, which has lower complexity and higher precision. Simulation results show that the CBL-DPD can effectively overcome the nonlinearity and memory effect of the wideband power amplifier (PA).**

Keywords—power amplifiers; digital predistortion; band limited; nonlinearity

I. INTRODUCTION

In order to satisfy the increasing demand on transmitting higher data rate and large capacity, the bandwidth of signals is continuously growing broader in the satellite communication systems. However, the power amplifier (PA) inherently suffers from nonlinearity and memory effects, which result in spectral broadening and adjacent channel leakage ratio (ACLR) performance degradation, and degrade the communication quality and performance. Digital predistortion (DPD) is one of the advanced linearization techniques that compensates for nonlinear distortion of the PA. Therefore, the higher speed analog to digital converter (ADC) will become a critical bottleneck in wideband DPD [1].

To solve this problem, several approaches were proposed. It can solve this problem by adding a bandpass filter in the feedback loop. However, it is difficult to accurately know the frequency response of the analog bandpass filter. The band-limited digital predistortion can effectively solve this problem [2]-[6]. In [2], a band-limited volterra series-based behavioral modeling approach was proposed, which allows us to accurately model a PA with band-limited input and output. In [4], Zhang et al. proposed a band-limited memory polynomial (BLMP) model, and LS method was used to extract the forward memory polynomial (MP) model with reduced sampling rate. Zhang et al. [5] proposed a DPD method based on PA modeling with restricted feedback bandwidth. Ma et al. [6] proposed a direct learning method with reduced bandwidth feedback, which is comparable to the full-rate system. The general DPD architecture for wideband PA systems with constrained feedback bandwidth is proposed in [3]. However, the band-limited DPD architecture is inconsistent with the feedback signal bandwidth of the output of the PA, which reduce the band-limited DPD linearization performance.

In this paper, we present a compensation band limited digital predistortion (CBL-DPD) architecture for wideband PAs with limited bandwidth feedback. Experimental results show that the proposed CBL-DPD architecture can effectively compensate the nonlinear distortion and memory effect of the wideband PA.

II. ADAPTIVE CBL-DPD SCHEME

A. System Architecture

This paper adds a low pass filter based on the traditional band-limited digital predistortion (BL-DPD). Due to the order of the low pass filter is too high, the calculation is too complicated. The order is too low, which will degrade the linearization performance of the DPD techniques. Therefore, this paper presents a compensation band limited digital predistortion (CBL-DPD) in fig. 1. Compared with traditional band limited digital predistortion (BL-DPD), the CBL-DPD adds a low pass filter (LPF) and an error compensation term that compensate the non-ideal pass-band ripple of the LPF. Thus, the CBL-DPD has a high accuracy with lower complexity.

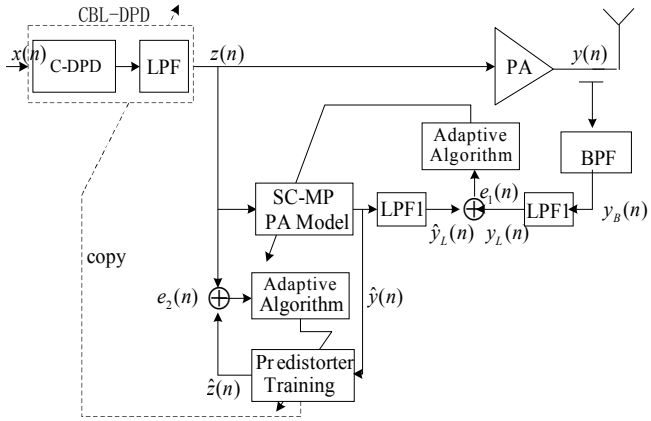

Fig.1 The diagram of CBL-DPD model

In order to the CBL-DPD do not need to know the exact frequency response of the analog BPF in the feedback path, this architecture consists of two branchs. The first branch is the LPF1 operation on both the feedback signal and the output signal of the SC-MP model to accurately estimate the SC-MP model. The second branch is applied in indirect learning for estimating CBL-DPD parameter.

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B. CBL-DPD Algorithm

The algorithm flow chart of CBL-DPD is shown in Fig. 2. Firstly, setting the error determinant threshold $|e_1(n)|=|e_2(n)|=1$, thus $|e_1(n)|=|e_2(n)|\geq e_0$, the adaptive algorithm estimates SC-MP parameters. Secondly, checking $|e_1(n)|$, if $|e_1(n)|<e_0$, the adaptive algorithm estimates CBL-DPD parameters. Then, checking $|e_2(n)|$, if $|e_2(n)|>e_0$, the adaptive algorithm continues DPD parameter estimation until optimal convergence. Otherwise, the algorithm is convergence, and the weight vector of the predistortion training is copied to the CBL-DPD. Finally, the output signal of the CBL-DPD gets through the power amplifier.

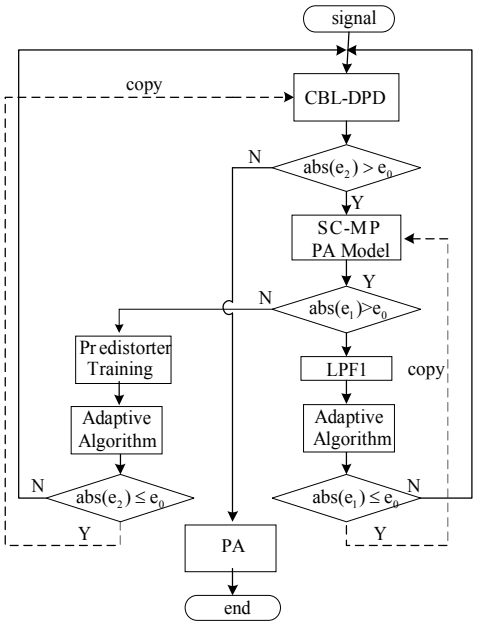

Fig.2 The diagram of CBL-DPD kernel model

C. SC-MP Model

Behavioral modeling is important for the implementation of DPD. Conventional DPD mostly use memoryless model, which suggests that the current output depends only on the current input. However, higher PAs may exhibit memory effects that can no longer be ignored in wideband applications. A simplified cross and memory polynomial (SC-MP) model was proposed in [7].

$$y_{\text{SC-MP}}=\sum_{k=1}^{N_1}\sum_{m=0}^{M_1}a_{km}\left|x(n-m)\right|\left|x(n-m)\right|^{k-1}+\sum_{\substack{p=1\\p\neq q}}^{M_2}\sum_{q=1}^{M_2}d_{pq}\left|x(n-p)\right|\left|x(n-q)\right|^{2} \quad (1)$$

where $y_{\text{SC-MP}}$ is the equivalent baseband signal of the output of the PA. N_1 , M_1 and a_{km} are the MP order, memory depth, and coefficients, respectively. M_2 and d_{pq} are cross items between memory times (CIMT) memory depth and coefficients.

D. CBL-DPD kernel Model

The DPD kernel function is contrary with the nonlinear characteristics of power amplifier. The digital predistortion linearization consists of two major steps. In order to ensure the linearization effect of the power amplifier, the output signal of digital predistortion must match the bandwidth of the feedback signal of the power amplifier. Therefore, this paper proposes the CBL-DPD kernel polynomial model to approximate the CS-MP model. The CBL-DPD kernel polynomial model has two parts. The first part is CBL-DPD kernel polynomial item, and the second part is error compensation item. The block diagram of the CBL-DPD kernel polynomial model is shown in Fig. 3.

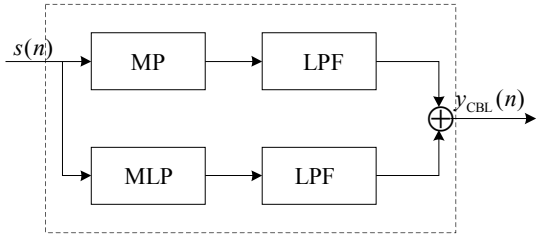

Fig.3 The diagram of CBL-DPD kernel model

The memory polynomial [8] mathematical expression can be represented as

$$y(n)=\sum_{k=1}^{K}\sum_{m=0}^{M}C_{km}\left|s(n-m)\right|\left|s(n-m)\right|^{k-1} \quad (2)$$

where $s(n)$ and $y(n)$ are the equivalent baseband signals of input and output of the traditional digital predistortion. K , M and C_{km} are the MP order, memory depth and coefficients, respectively.

Then, we insert an band-limited function for traditional BL-DPD to make the bandwidth of the output signal of the DPD approach the feedback signal. The BL-DPD kernel mathematical can be represented as

$$y_{BL}(n)=\sum_{l=0}^{L}h_l y(n-l) \quad (3)$$

where $y_{BL}(n)$ denotes the output signals of the BL-DPD， h_l and L are coefficients and order of the LPF, respectively, namely

$$y_{BL}(n)=\sum_{k=1}^{K}\sum_{m=0}^{M}\sum_{l=0}^{L}r_{lml}\left|s(n-m-l)\right|\left|s(n-m-l)\right|^{k-1} \quad (4)$$

where r_{lml} is the coefficient of the BL-DPD kernel.

The good performance of the BL-DPD depend on the order of the LPF. The number of the LPF order is higher, the performance of the BL-DPD is better. But it is increase the complexity of the DPD system. In order to reduce the order of the LPF of the BL-DPD, we use memoryless polynomial (MLP) model to make up for lost information, which is affected by the in-band ripple of low order LPF. The MLP can be written as