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Robust low power DC-type shift register circuit capable of compensating threshold voltage shift of oxide TFTs ☆

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ABSTRACT

This paper proposes an oxide TFT DC-type shift register that consists of eleven TFTs and one bootstrapping capacitor. The proposed circuit connects drain nodes of large size pull-up TFTs of output drivers to positive supply voltage instead of alternating clock signals for low power consumption. In addition, a robust internal inverter capable of maintaining the high voltage level of the output over the large positive threshold voltage shift by bootstrapping is implemented. For a 120 Hz Full-HD display, the SPICE simulation estimates the clock power consumption of the proposed DC-type circuit as 0.56 mW at 32 shift registers and ensures the robust operation over the wide range of threshold voltage shift from −4 V to 10 V.

1. Introduction

In mass production of active matrix flat panel displays, integrated gate drivers have been widely employed due to simple structure and low product cost [1–5]. However, these thin film transistor (TFT) circuits have the disadvantage of high power consumption caused by high operating voltage and large circuit area. Above all, the clock power takes the biggest part of total power consumption because the alternating clock signals at the high frequency are connected to all shift registers of a gate driver circuit, that is, the huge capacitive load. Until now, there are two ways to reduce the clock power consumption. One method is to reduce the operating frequency by increasing the number of clock signals [6]. However, whereas the power consumption of each clock is lowered, the overall clock power consumption remains similar due to the increased number of clock signals. The other approach is to decrease the capacitive load of clock lines by employing the output stage of a direct-current (DC) type in each shift register circuit [7–10]. Because the substantial portion of the capacitive load in conventional shift registers is made up by gate-drain overlap capacitance of large-size pull-up TFTs, the capacitive load of clock signals can be remarkably reduced by connecting the DC supply voltage, instead of clock signals, to pull-up TFTs.

We have already reported the DC-type shift register circuit with low temperature poly-silicon (LTPS) TFTs [11] that achieved the clock power reduction by 97% compared to the conventional one. On the other hand, the same architecture does not work properly in the backplane of oxide TFTs due to the depletion mode characteristic and positive threshold voltage shift [12,13]. This paper proposes a low power oxide TFT DC-type shift register that copes with both issues of depletion mode TFTs and positive threshold voltage shift.

2. Proposed programmable shift register circuit

Fig. 1 shows the previous LTPS TFT DC-type circuit composed of nine TFTs (N1–N9) and one bootstrapping capacitor (Cap) [11]. If this previous circuit is implemented at an oxide TFT backplane, some problems take place due to depletion mode TFTs and positive threshold voltage shift. The gate-source voltage of 0 V is not able to turn N3 off completely in the depletion mode. Since Q[n] cannot retain the floating state, the bootstrapping effect is not generated properly. In addition, the positive threshold voltage shift in pull-down TFTs (N7, N9) leads to the lifetime degradation of the circuit owing to long time positive bias stress.

To cope with these two issues, a robust oxide TFT DC-type shift register circuit is proposed with eleven n-channel oxide TFTs

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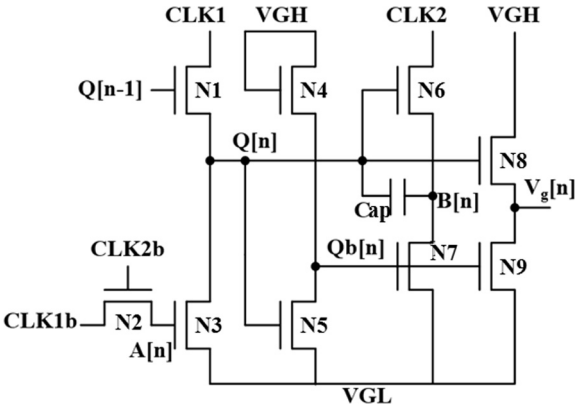

Fig. 1. Previous LTPS TFT DC-type shift register [11].

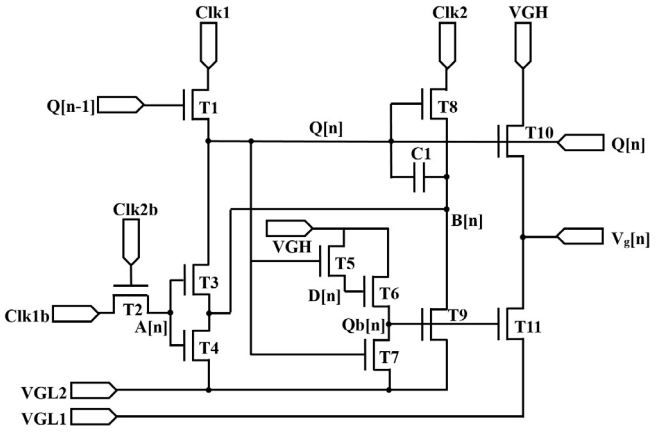

Fig. 2. Proposed Oxide TFT DC type shift register.

(T1–T11) and one bootstrapping capacitor (C1) as illustrated in Fig. 2. Two different low voltage levels (VGL1, VGL2) and a series-connected two-transistor (STT) structure of T3 and T4 [14] are applied to address the depletion mode issue. VGL2 is set to the lower voltage than VGL1. In the depletion mode, zero gate-source voltages cannot turn TFTs off completely leading to the increased power consumption or the malfunction of the circuit. Especially, because large size T10 and T11 in the output stage significantly can increase the power consumption, low levels of their gate and source voltages are generated in VGL2 and VGL1, respectively. Consequently, the negative gate-source voltages allow TFTs to be turned off completely. Additionally, STT enables turning T3 off by connecting the high voltage of B[n] to the source node. To extend the lifetime, a new internal inverter composed of T5, T6, and T7 keeps the high voltage level of Qb[n] at VGH regarding the wide range of threshold voltage variation and enables T9 and T11 to operate well even at the large positive threshold voltage shift. When Q[n] is high, the inverter circuit operates exactly in the same way of the normal diode-connected load inverter. However, when Q[n] is pulled down, D[n] turns to be a floating state of high voltage that is boosted to higher level by the rising transition of Qb[n]. Therefore, Qb[n] is allowed to reach to VGH unlike the conventional diode-connected load inverter.

As a timing diagram depicted in Fig. 3, four clock signals (Clk1, Clk2, Clk1b, Clk2b) with a duty ratio of 50% are in use similarly to the previous LTPS TFT circuit. Clk2 is a delayed signal with respect to Clk1 while Clk1b and Clk2b are the out-of-phase clocks over Clk1 and Clk2 respectively. The operation of the proposed shift

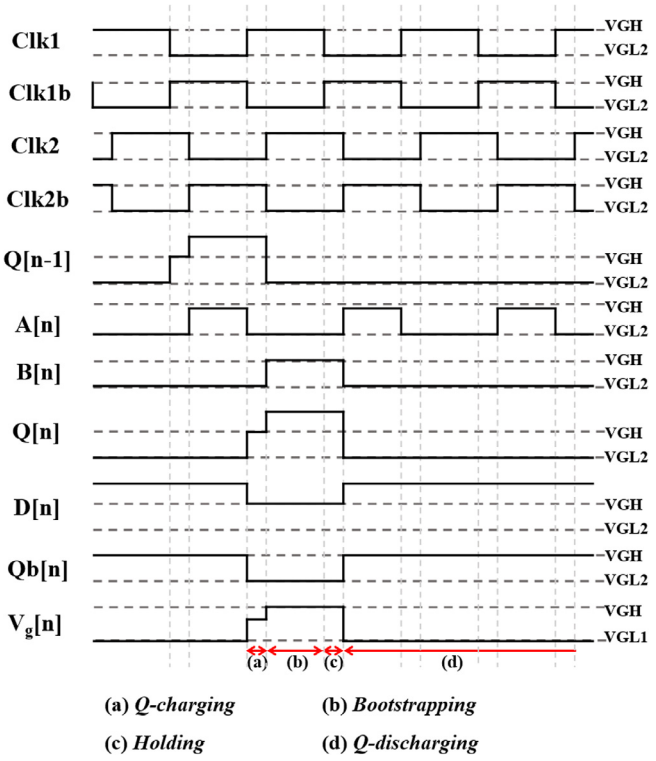

Fig. 3. Timing diagram of a proposed oxide TFT DC-type shift register.

register circuit is explained with four steps of *Q-charging*, *Bootstrapping*, *Holding*, and *Q-discharging* as follows.

In the *Q-charging* step as illustrated in Fig.4(a), Q[n] is charged to the VGH level by Clk1 through T1 that is fully turned on by the boosted Q[n − 1] of a previous stage. Meanwhile, Clk1b sets A[n] at the low level via T2 to cut off the path between Q[n] and VGL2 by turning T3 and T4 off. At the same time, T9 and T11 are turned off by Qb[n] that is pulled down to VGL2 by an internal inverter of T5, T6 and T7 with the high voltage of Q[n]. Since Q[n] of VGH turns T8 and T10 on, V_g[n] is pulled up to the lower level than VGH by the threshold voltage of T10 and B[n] is maintained at VGL2 by Clk2.

During the *Bootstrapping* step, Q[n] becomes a floating node of VGH since the low voltages of Q[n − 1] and A[n] turn T1 and T3 off completely due to source and drain nodes connected to high voltages close to VGH. Therefore, the positive transition of Clk2 makes the same transition on B[n] that boosts Q[n] up to the higher voltage than VGH through C1 by the bootstrapping effect. This higher Q[n] enables V_g[n] to reach to VGH as described in Fig.4(b). The voltages of other nodes are equivalent to the *Q-charging* step.

For the *Holding* step, all nodes are maintained at the similar voltages to the *Bootstrapping* step. Even though there might be a leakage from Q[n] to Clk1 via T1, the short period of this step does not make any serious impact on the voltage level of Q[n]. Therefore, V_g[n] stays at the high level of VGH as depicted in Fig.4(c). In this step, the overlap between V_g[n] and V_g[n + 1] takes place.

At the last *Q-discharging* step shown in Fig.4(d), A[n] is switched to the high level to turn T3 and T4 on with high level Clk1b and Clk2b, which causes Q[n] to be pulled down to VGL2. Then, the low level of Q[n] sets T8 and T10 to be off and turns T5 and T7 off in the internal inverter, resulting in the bootstrapping on floating D[n] through the gate-source overlap capacitor of T6.