INTEGRATION the VLSI journal 60 (2018) 25–38

Contents lists available at ScienceDirect

INTEGRATION, the VLSI journal

journal homepage: www.elsevier.com/locate/vlsi

Optimum transistor sizing of CMOS logic circuits using logical effort theory and evolutionary algorithms

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ARTICLE INFO

Keywords:
Digital VLSI
CMOS logic circuits
Optimization
Logical effort theory
Heuristic algorithms
Power-delay-area product

ABSTRACT

Most existing methodologies use either Logical Effort (LE) theory or stand-alone optimization algorithms for automated transistor sizing of CMOS logic circuits. LE theory optimizes a logic circuit only with respect to speed while it completely ignores power and area. Whereas heuristic algorithms when used as a stand-alone approach for optimization lead to huge computational effort since there is no predefined technique to apply constraints on transistor sizes in order to limit the design space for target specifications. The problem has been resolved in this paper by utilizing delay sensitivity factor based on LE theory proposed by Alioto et. al. [1] for estimating the highest operating speed of a logic circuit and determining the upper bound on the size of transistors. Recently proposed heuristic algorithms viz. Interior Search Algorithm (ISA) [2] and Gravitational Search Algorithm (GSA) [3] have been utilized further to converge towards minimum power-delay-area product (PDAP). Simulation results for various test circuits indicate upto 35.1% and 63.8% improvement in power-delay product (PDP) and PDAP respectively in 130 nm/1.2 V TSMC CMOS technology. PVT analysis and Monte Carlo simulations have been used to further validate the effectiveness of the proposed methodology.

1. Introduction

Optimal gate sizing of transistors is amongst the fundamental problems in VLSI circuit designing. Size of transistors in any CMOS logic circuit directly affects its performance in terms of speed, power dissipation etc. An efficient digital CMOS integrated circuit (IC) presents an optimal trade-off between speed and power dissipation. For circuits which constitute small number of transistors, manual transistor sizing is possible. But the ever increasing demand for portable electronic devices with enhanced features has triggered design of digital CMOS circuits with very high complexity. As a result, the task of designing and optimizing these circuits for target specifications has become extremely cumbersome. This necessitates inclusion of automation in the design and optimization flow of CMOS logic circuits such that least amount of manual effort is involved in optimizing smaller logic blocks with varying specifications for design reuse in high complexity IC design.

The most important design parameters in CMOS logic circuit design are delay, power and area. Numerous methods have been proposed in the past to carry out optimization of these parameters. Transistor sizing techniques with focus on reduction of delay and area have been demonstrated in [4–6]. Sapatnekar et. al. [7] have demonstrated an efficient convex optimization technique to find minimum area of a circuit for a target delay constraint by analyzing the area-delay tradeoff. However, the application of the technique is limited to only combinational circuits which is a serious drawback. A non-convex polynomial optimization method has been presented by Lui et. al. [8] which guarantees convergence to globally optimal solution with superior computational efficiency in comparison with other traditional non-linear programming (NLP) based techniques. However, the technique is used for only analog CMOS circuits. Berkelaar et. al. [9] have proposed a method which considers design parameters in the form of linear equations and constraints in terms of linear inequalities.

Logical Effort (LE) theory [10] is one of the most widely used methods in the literature for optimization of digital CMOS circuits. LE theory is based on linear delay modelling and consequently exhibits a deviation of 15 – 20% from theoretical delay estimations when circuits are realized on chip. Further, it optimizes circuits only for delay and completely neglects power and area considerations. Additionally, input signal slope variations are not taken into account while estimating circuit delay using LE theory. A solution to tackle this issue has been reported by Wang et. al. in [11]. Nonetheless, LE theory provides a quick estimate of minimum delay for both single and multi-stage circuits and it also evaluates the best number of stages in a multistage circuit for highest operating speed.

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http://dx.doi.org/10.1016/j.vlsi.2017.08.003
Received 22 October 2016; Received in revised form 14 May 2017; Accepted 7 August 2017
Available online 15 August 2017

In recent times, several researchers have utilized heuristic techniques to optimize CMOS circuits. Aezinia et al. [12] have demonstrated optimization of modified hybrid latch flip-flop (MHLFF) using Genetic Algorithm (GA) for minimum PDP. Gupta et. al. [13] have employed GA and ACO to obtain optimal transistor width sizes by minimizing PDP. Rogenmoser et. al. [14] have utilized Monte Carlo scheme and GA based technique to obtain optimal sizes of CMOS circuits concluding that Monte Carlo scheme is advantageous for small circuits whereas GA is more efficient for circuits with relatively high complexity. Slowik & Bialko have minimized gate count, transistor count and circuit delay using GA in [15]. Jalali et. al. [16] have optimized 16-bit carry skip adder for optimal speed and power by utilizing GA and multi-threshold CMOS. Thakker et. al. [17] have utilized hierarchical particle swarm optimization (PSO) to size low-power analog circuits. Results have been compared with circuits optimized through PSO and GA. Johari et. al. [18] have achieved minimum delay of 8-stage full adder circuit by utilizing mutative particle swarm optimization (MPSO) which is guided by LE theory. High convergence rate to optimal solution was indicated by the results obtained. Some of the researchers have used metamodeling as an effective way for automated optimization of mixed-signal designs but they lack in estimation of upper bound on transistor sizes based on simple back of the envelope calculations leading to complex design procedures and high computational effort [19,39]. Ultra low power design using sub-threshold standard cell library still utilizes LE theory for speed optimization of logic gates [20].

In this paper, we have adopted Interior Search Algorithm (ISA) [2] and Gravitational Search Algorithm (GSA) [3] in order to optimize different circuits (both combinational and sequential) in a three dimensional design space viz. power, delay and area by minimizing PDAP on automated basis. Moreover, this 3-dimensional optimization problem is virtually reduced to a 2-dimensional one by utilizing a LE theory guided methodology. Initially, LE theory is used for solving the dual purpose of determining the optimal speed and upper bound on transistor sizes. This is extremely useful in curtailing the design space and minimizing the computational effort early in the circuit design cycle. In the subsequent stage of optimization, the objective function (PDAP) is formulated such that ISA/GSA is focussed to converge towards minimum power-area product while the delay component is fixed at the minimum value obtained from LE theory. Additionally, constraint on upper bound of transistor size is also obtained from LE theory. The optimization process has been automated by developing MATLAB-SPICE interface. The algorithms have been implemented in MATLAB (R2013a version) while the objective function is evaluated on an iterative basis by keeping SPICE in the loop. The main benefit of using the proposed approach lies in the fact that power and area aware digital circuits can be realized on an automated basis without compromising the maximum speed obtained traditionally from the LE theory. This applies to automated full custom design of digital circuits for implementing critical low power sections in ASIC design flow and mixed signal systems. Automated full custom design globally optimized in power-delay-area design space will increase the chip performance and reduce the chip-turn around time.

The rest of the paper is organized as follows. Section 2 describes the functionality of ISA and GSA. The performance of both ISA and GSA has been validated in Section 3 by demonstrating optimization of a test function towards global minimum. Section 4 describes the proposed LE theory guided optimization approach using ISA or GSA. This is a hybrid approach and will be referred to as LE-ISA and LE-GSA throughout the rest of the paper depending upon the algorithm used with LE theory for the overall optimization process. Section 5 highlights the simulation results obtained by employing a variety of test circuits and finally conclusion is summarized in Section 6.

2. ISA and GSA algorithms

2.1. Description of ISA

ISA is a meta-heuristic algorithm proposed by A. H. Gandomi in 2014 [2]. It is based on the aesthetic techniques used in Persian art for interior decoration and design. The algorithm utilizes the Persian practice of placing mirrors to enhance the beauty of objects to reach an optimal solution. Each agent in ISA is a potential solution to the optimization problem. The fitness value of the agent is evaluated based on the position of the agent in the search space. Each agent can either be subject to exploration or exploitation. The user has direct control over the probability of an agent choosing exploration or exploitation. An agent which is far from the optimal solution is subject to exploitation, which leads to re-initialization of the agent in the search space using Eq. (1).

$$x_i^j = LB^j + (UB^j - LB^j) \times r_2 \tag{1}$$

For an agent considered closer to the optimal solution, we use the Persian mirror placing approach to reach optimal solution using Eqs. (2) and (3)

$$x_{m,i}^j = r_3 \times x_i^{j-1} + (1 - r_3) \times x_{gb}^j \tag{2}$$

$$x_i^j = 2 \times x_{m,i}^j - x_i^{j-1} \tag{3}$$

where, LB is the lower bound, UB is the upper bound, x is the position of the current agent, x_m is the position of mirror (used to find position of mirror element), x_{gb} is the position of best agent in the iteration, i is the agent index, j is the current iteration, and r_2, r_3 are the random variables lying between 0 and 1.

ISA has been used for engineering optimization problems, like tension/compression spring design, pressure vessel design, 72 bar space truss design [2] etc. Kumar et. al. have used ISA in wideband digital differentiator design problem [21]. A modified form of ISA has also been used in solving an integer order Rossler's chaotic system [22].

2.2. Description of GSA

GSA is a heuristic algorithm originally proposed in 2009 by Rashedi et. al. [3]. It is a swarm-based algorithm that is based on the law of gravitation. Every object in the search space is characterized by two parameters, namely position and mass. The position of the object indicates the solution and its mass is used for the performance evaluation. The position of the object with higher mass will signify a better solution than the position of an object with lower mass. The object with higher mass (better solution) attracts the objects with smaller mass (poorer solution) as time passes, thus converging to an optimal solution. The force of attraction is calculated for each agent based on all other masses in the system. Acceleration of the agent is calculated based on the force and is further used to calculate the velocity and position of the agent using following equations.

$$F_{ij}^d(t) = G(t) \times \frac{M_{pi}(t) \times M_{aj}(t)}{R_{ij}(t) + \epsilon} \times (x_j^d(t) - x_i^d(t)) \tag{4}$$

$$F_i^d(t) = \sum_{j=1, j \neq i}^{N} rand_j F_{ij}^d(t) \tag{5}$$

$$a_i^d(t) = \frac{F_i^d(t)}{M_{ij}(t)} \tag{6}$$

$$v_i^d(t+1) = rand_i \times v_i^d(t) + a_i^d(t) \tag{7}$$