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# A novel switchable pin method for regulating power in chip-multiprocessor

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ABSTRACT

Transistor scaling has allowed a large number of circuits to be integrated into integrated circuit (IC) chips implemented in nanometer CMOS technology nodes. However, dark silicon which signifies for under-utilized circuitry will become dominant in future chips due to limited thermal design power (TDP). Furthermore, large voltage loss due to complex routing and placement will also degrade the performance of ICs. In addition, effectively managing power dissipation in a packaged chip is one of the major issues of IC design. Previous work done by our group mainly focused on RCL simulation and elementary IC simulation, this work not only builds on power delivery network (PDN), but also designs switchable pin working for two cores at the layout level. The essence of our idea is to supply power to the chip using traditional I/O pads. In order to balance power supply and I/O bandwidth, we set several groups of parallel switchable pins between the core and memory such that I/O pads can dynamically switch between two modes which are data transmission and power supply. To remove the risk that large current going through I/O pad breaks down the pad frame, we redesigned traditional I/O pad to operate in bi-direction. Using TSMC CMOS 180 nm process for the design and simulation, our test results show that the proposed switchable pin can well compensate voltage loss in chip multiprocessor, and transfer time of two modes is very short. For data transmission, we perform a sensitivity study to explore the impact brought by switchable pins. Our simulation results demonstrate that performance degradation is in acceptable range when the switchable pins are added to the chip-multiprocessor.

## 1. Introduction

Efficient circuit and hardware implementation are critical to achieve high performance computing. Growing clock frequency and design complexity will inevitably increase processor power dissipation. For emerging nanometer silicon MOSFETs, quantum effects are dominant, and thus the sub-threshold leakage [1] and resulted heat dissipation are the critical problems of future IC development. Limited thermal design power (TDP), dark silicon [2,3] which refers to frequency drop or even turning-off of transistors will happen in future chips and will counteract the purpose of transistor scaling. From the perspective of voltage regulation, complex routing and placement will potentially bring the irregular power supply to each block in a chip, which will obviously affect the reliable operation of the chip.

Effective power distribution plays an important role in IC chip design [4]. Extensive work has been done on power management in both circuit and architecture areas. On-chip and off-chip voltage regulator have been designed [5,6], which can robustly manage power modes according to different workloads. Lots of passive devices are integrated with packaged chips and motherboards, however, it is at the cost of bringing area and complexity. In [7], an architectural concept has been proposed where the chip multiprocessor serves multi-functions in portable devices. The sub-core is designed in such a way that it can largely enhance the utilization ratio of a single chip. In [8], an extreme turbo technique is demonstrated where a core runs under the ultra-fast speed in short time and then under-clock for a while at cost of a non-conventional cooling device with phase change materials.

The present work is based on our earlier work [9–11]. Previous works proposed a switchable pin concept for an efficient power delivery which has been simulated in both RCL and simple IC level. The method is to fully use I/O pins with their pads to convert them as a group of power pads to compensate voltage loss in chip. This work use specific PDN simulation to build proper PCB environment letting the switchable pins reliably work in chip multiprocessor with two sub-cores with the help of clock block. We explore also the voltage compensation due to switchable pins, chip cost brought by switchable pins and signal integrity negatively influenced by switchable pins.

The contributions of this work include: 1) we analyze the voltage loss due to long global wires under the rules of routing/placement in current VLSI chips. The trend of voltage loss in chips designed in sub-

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nanometer process technologies is anticipated, 2) with the switchable pins added, the interface between core and memory is needed to be modified to keep proper signal integrity, thus we model a power delivery network (PDN) and build a specific PDN with proposed switchable pins for our design. Our PDN is guided by the rules of proper PCB design and extracted parameters in IC fabrication process (TSMC 180 nm), 3) we modify traditional I/O pad to meet the requirement of current to boost IC chip going through the pad frame since parts of I/O pads need to be used as power pads and overlarge current might break down the pad frame, 4) our circuit design is based on a microprocessor including two sub-cores and a group of memory chips in layout level as the platform. Design of interface on PCB is based on PDN modeling and for controllable switchable pins, a specific clock circuit is introduced and 5) we verify that switchable pins can well compensate voltage loss with low cost. We also perform a sensitivity study to explore the impact brought by switchable pins including signal integrity under different frequencies.

The rest of the paper is organized as follows. Section 2 presents the analysis of voltage loss in chips. Section 3 presents the concept of switchable pin and its PDN modeling. Section 4 is on the modification of I/O pad. Section 5 is our circuit design implementing switchable pin and relative test report. The summary is presented in Section 6.

## 2. Analysis of voltage loss

Finite width of wire, contact resistance and complex routing will cause voltage loss in chips. Previous theoretical study has proved that voltage drop can influence the performance of data transmission [12]. The current IC fabrication allows multi-layer process in silicon wafers to release the pressure of chip layout. But complex interconnect/contact and inductor effect under high frequency still degrade voltage distribution in chips. Fig. 1 shows a cross-section view of power supply interconnection from multiple layers. For a global metal wire in a chip, the voltage loss can be described by the following equation:

$$V_{loss} = \sum_{i=1}^{m-1} R_{c\_i} i_w + \rho_w \frac{l}{w} i_w + Z_L i_w \quad (1)$$

where $m$ is the number of metal layers, $R_{c\_i}$ is the contact resistance, $i_w$ is the current flowing through the wire, $l$ and $w$ are the length and width of the global wire, respectively. $Z_L$ is the impedance of inductor in global interconnection. The three terms in Eq. (1) reflect the voltage loss contributed by contacts, wire resistance, inductor effect under high frequency, respectively.

To estimate the voltage loss in chips, we make following considerations: a) The parameters of fabrication process we use for estimation is Predictive Transistor Model (PTM) [13]; b) The global wire serving for power supply is straight without complex rotation, which means we ignore mutual inductance effect between neighboring wires. The parameters of interconnect for the selected fabrication process are extracted as in [14]; c) We consider 10 multi-layers in a chip. The top and bottom layers are used as global layers and layer supplying power to sub-block, respectively; d) The voltage loss due to inductor at higher

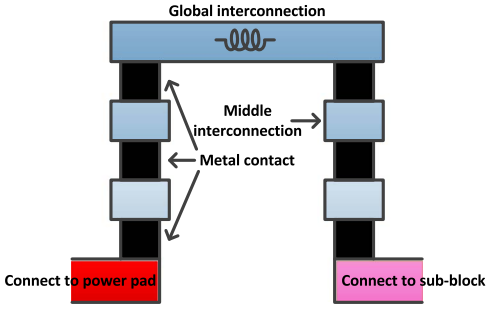


**Fig. 1.** Cross-section view of power supply interconnection from multiple layers.

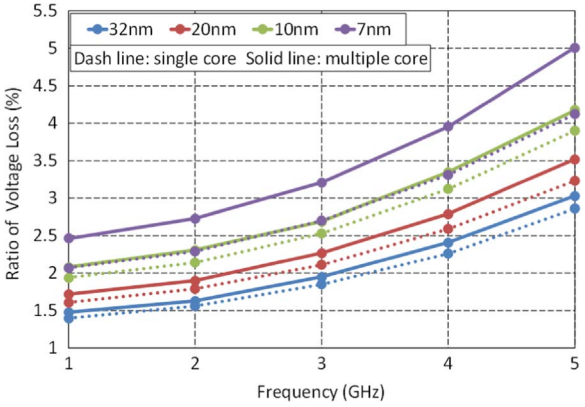


**Fig. 2.** Voltage loss ratio in various fabrication processes.

frequencies are dynamic loss and static loss as well [15]. Here we only focus on static loss, which means for the loss due to inductor effect, absolute value of impedance is taken into estimation without the consideration of phase; e) We select a virtual core which has 100 million transistors. For each transistor, we use minimum dimension in the selected process. Considering gaps between adjacent transistors/subblocks, the area of the virtual core is close to 1.2×100 million transistors. For a single transistor, DRC rules cannot be neglected, we explore currently mainstream layout of a single transistor with the strategy of saving area, the area of a single transistor is $(1.5\times l)\times(3\times w)$; f) Largest voltage loss happens in the geometrical center of the virtual chip; and g) For a virtual chip multiprocessor, we set that there are 2, 4, 6, 8 virtual cores in a chip multiprocessor corresponding to 32 nm, 20 nm, 10 nm, and 7 nm fabrication processes, respectively.

Guided by above considerations from (a) to (g), we can calculate the voltage drop in the virtual single core and chip multiprocessor for various sub-nanometer processes, as shown in Fig. 2. We observe that the voltage loss increases with the frequency due to inductance effect. It is anticipated that if emerging chips work under ultra-high frequency, or have too many layers, voltage loss will be continuously increased. Another issue which needs to be analyzed is the relationship between voltage loss and transmission time of signals in chips. In this work, we mainly study how voltage loss influences rise and fall times, which are significant factors determining signal transmission. The mathematical relationship can be shown as follows [16]:

$$t_f = t_r = \frac{2C_L}{\beta(V_{DD} - |V_{TH}|)}\left[\frac{|V_{TH}| - 0.1V_{DD}}{V_{DD} - |V_{TH}|} + 0.5\ln\left(\frac{19V_{DD} - 20|V_{TH}|}{V_{DD}}\right)\right] \quad (2)$$

Current digital VLSI is based on static logic and the load capacitance is mostly contributed by the equivalent gate capacitance of the next stage. Fig. 3 shows the growth rate of fall/rise time calculated at 1 GHz using PTM under the influence of voltage loss which increases with the increase in frequency. It can be concluded that if no voltage calibration is used for VLSI chips, voltage drop will seriously influence this performance. The mainstream strategy to avoid this problem is embedding in-chip a voltage regulator. However, this method is at a cost of power dissipation and real estate.

## 3. Concept of switchable pin and its power delivery model

Normally, a complex function digital VLSI chip has one power pad, one ground pad, clock pad, and several data pads used for writing or reading. This feature can maximize the bandwidth of data transmission for a specific package. But only one pair of pads used for power supply cannot guarantee each sub-block to work under a perfect voltage as analyzed in the last section because of complex route and placement. If we set more pads as power pads, it can be seen that the performance of power supply in multi-power pads will be enhanced compared to in a