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Aging signature properties and an efficient signature determination tool for online monitoring

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ABSTRACT

Increased reliability problems in deep sub-micron CMOS technologies have led to a dramatic decrease of lifetime of analog integrated circuits. To palliate this problem, several reliability-aware design approaches have been developed. Reconfigurable circuit design is one of those approaches, which is based on reconfiguring the circuit considering degradation in circuit performances. *Sense & React* (S & R) approach is the well-known reconfigurable design approach, where degradation in circuit performances are sensed and a pre-established recovery operation is applied to heal the circuit. In practice, indirect measurements are preferred during sense operation, in which electrical quantities are measured in order to determine time to recovery. Determination of the time to recover is the most critical part of a S & R system. One or more circuit variables are selected out of all measurable circuit quantities. The selected signature should have some attributes to be used as the aging signature to reduce the measurement cost. However, efficient aging signature properties have not been defined in the literature yet. Moreover, the designer determines the aging signature manually by performing an iterative search and evaluation on aging simulation results, and there is no tool to ease this time consuming process. This paper clearly describes the aging signature properties and proposes an automatic signature selection tool that determines the most efficient signature for sense operation.

1. Introduction

The scaling difference in CMOS technology between the supply voltage and feature size, which has been more aggressively scaled down, causes an increase in power density and higher electric field in the gate dielectric [9]. As a result of increased internal electrical stress on devices, time-dependent reliability problems, such as Hot Carrier Injection (HCI), Bias Temperature Instability (BTI), and Time Dependent Dielectric Breakdown (TDDB) have become more severe in advanced technology nodes, which dramatically result in circuit lifetime reduction. Therefore, aging analysis has become a part of the conventional design flow in order to observe the aging effects on circuit performance and redesign the circuit if the targeted lifetime is not achieved.

Aging-aware circuit design approaches can be classified under two main categories: precaution-based and healing-based approaches. Over design is one of the precaution-based approaches, in which the circuit is designed considering aging effects and a safety margin for certain circuit specifications is left by selecting a design point far enough from the optimal region as depicted in Fig. 1. As a result, over design suffers from a trade off between lifetime and other design specifications, such as power consumption and chip area [12].

Robust design is the other precaution-based approach, in which a more robust design point is selected from the feasible design space as shown in Fig. 1. The selected circuit operates properly even if aging takes place. However, finding such a design point over the whole design space is highly challenging in addition to being a very time consuming process. Furthermore, some circuit specifications may have to be sacrificed for the sake of reliability. In both approaches, the designer should re-evaluate the design and determine the trade-off between circuit performance and lifetime [13].

Contrary to precaution-based techniques, reconfigurable circuit design is the well known healing-based approach, which is based on recovery of circuits after degradation occurs [11,7]. Reconfigurable circuit design does not suffer any performance trade-off during the design process and promises a fully recovery of circuit as depicted in Fig. 1. *Sense & React* (S & R) approach is a very popular reconfigurable design technique, which is based on sensing the degradation in circuit performances and activating the recovery operation when any violation in any circuit specification is detected [8,1]. Therefore, the time to recovery, which is determined by the sense operation, is highly critical and should be

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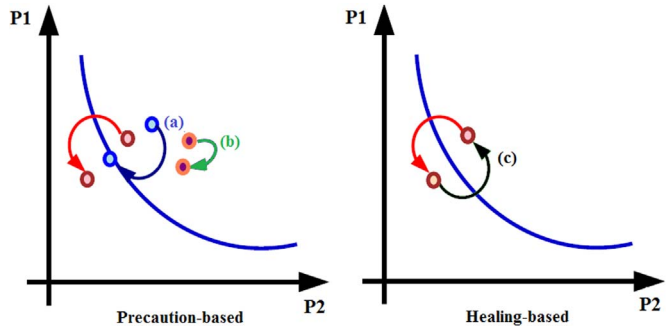

Fig. 1. Circuit design approaches against aging phenomena: (a) Over design, (b) Robust design, and (c) Reconfigurable design.

carefully considered during the design process. Sense operation is performed via online monitoring circuits [6]. Since it is very expensive to measure the changes in circuit performances directly, indirect measurements are preferred, where measurable quantities, such as node voltages, branch currents, and phase/frequency of a signal are measured [4,15,10]. These are then mapped to the circuit performance changes and the aging signature is selected out of among all candidate signatures. However, determining efficient signatures is not trivial, on the contrary quite a challenging process, since an efficient signature should have certain properties, which have not been clearly defined in the literature.

Traditionally, signature selection is performed by the designer in an iterative manner. At first, an aging analysis is performed and a signature-specification space is obtained. Then, the designer evaluates all candidate signatures one by one and determines the most efficient signature considering the measurement cost and accuracy. However, this analysis is highly inefficient and very time consuming, and to our best knowledge, no other procedure has been proposed for this process. This paper examines the efficient signature concept in the context of S & R approaches, clearly describes the properties of the efficient signature, and proposes a novel signature selection procedure. Furthermore, a novel tool that automatically determines the most efficient aging signature for online monitoring is developed, which can substantially reduce the design time of S & R systems.

Remainder of the paper is as follows. In Section 2, a fundamental background is provided, where the S & R approach is briefly explained and the properties of the efficient signature is described. In Section 3, the proposed procedure and the developed tool are explained in detail. Results of two different test circuits for two different types of signatures are provided and discussed in Sections 4 and V. Finally, the paper is concluded in Section 6.

2. Background

2.1. Sense and react

A general block diagram for a S & R system is provided in Fig. 2. The first operation is called “Sense”, in which a change in a certain circuit signature is detected via a sensor circuit. In general, the type of the sensor depends on the application. Node voltages, branch currents, and phase/frequency of a signal can be used as aging signatures. While voltage and phase/frequency quantities can be detected directly, a sampling circuit is required to sense the change in the current. Typically, current mirrors are used to sample the current flowing in a branch. However, the design of a current sampling circuit is highly critical since the aging of the mirroring transistor causes inaccurate sampling, which may disrupt the whole recovery mechanism. Therefore, one should consider this problem when a current based detection is utilized.

After a degradation signal is generated by the sensor circuit, the system reacts by applying the pre-determined recovery operation. Conventionally, there are three types of recovery operations: Adaptive biasing, adding supplementary transistors/blocks, and replacing aged transistors/blocks with fresh ones.

A S & R system can be designed in two different manners: continuous time and discrete time. The continuous time approach provides immediate response capability, which is very important especially for devices exposed to unexpected extreme environmental conditions (aerospace applications, etc). However, continuous time evaluation brings additional power consumption since all the supplementary circuits would always be active as well as the actual circuit. On the other hand, the discrete time approach requires an external enable signal to activate the sense and recovery blocks and has a delayed response to instantaneous changes. Since circuits are active only for a very short duration, there would be almost no extra power consumption in this case.

2.2. Efficient aging signature properties

To reduce the measurement cost, the number of aging signatures

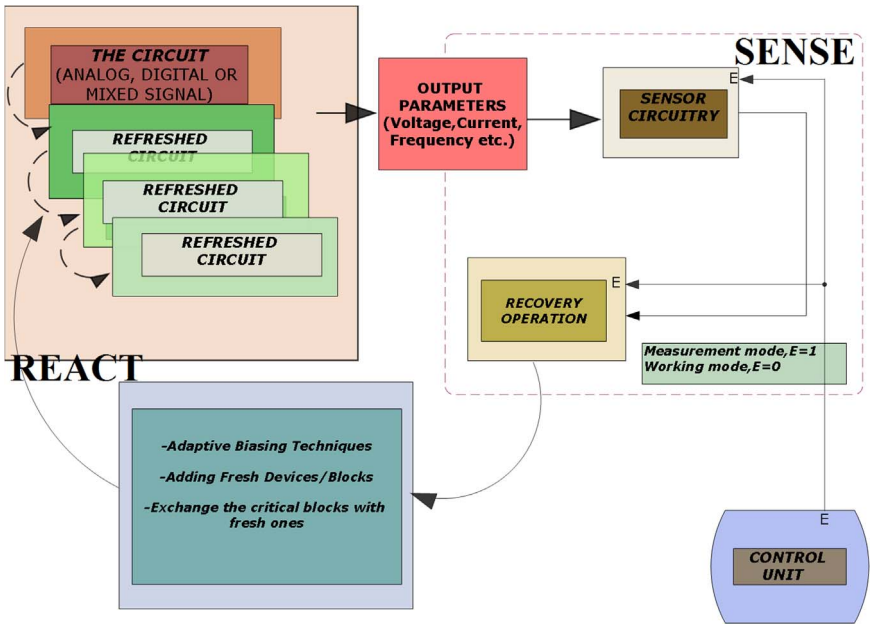

Fig. 2. A general scheme for Sense and React approch.