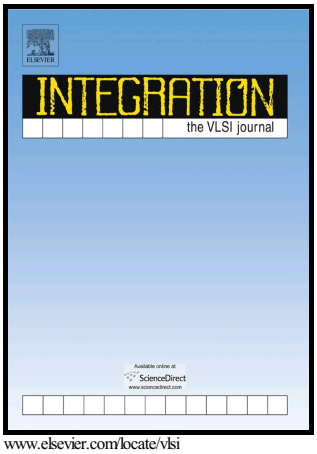

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A Novel Test Compression Algorithm for Analog Circuits to Decrease Production Costs

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Abstract

Minimizing the manufacturing test time for ICs is one of the main keys to reducing the product cost. We introduce a methodology for automated test compression for electrical stress testing of analog and mixed signal circuits. This methodology optimally extracts only portions of a functional test that electrically stress the nets and devices of an analog circuit. We model test compression as a problem of optimizing functional of the transient response. We present a random tree based approach to find the minimum for these computationally hard integrals, which corresponds to the optimally compressed analog test. We demonstrate with an op-amp, VCO, and CMOS inverter that the method consistently reduces the length of each test by an average of 93%. Our technology can compress tests in the presence of process variation and utilize parallel processing to speed up the compression algorithm.

Keywords: Analog Testing, Random Tree Search, Functional Optimization, Stress Testing

1. Introduction

1.1. Problem and Motivation

With the movement towards system-on-chip (SoC) ICs, the number and diversity of mixed-signal circuits on a die has increased significantly in the form of different high-speed IOs, sensors, power, and clocking circuitry. Among these, analog components are tested using specification-based functional tests with some design-for-test (DFT) features built in.

The steps in manufacturing test are broadly categorized into wafer/sort testing, packaged part class test (using functional and structural tests) which includes stress testing/burn-in, and system testing [25]. These steps need to be performed on every part that is shipped, resulting in a high volume of parts to be tested. To achieve fast product ramp to customers, the test time per part should be small, to the order of a few seconds. Although short test times can be achieved by increasing the test equipment, this is not a preferred choice due to the sharp increase in capital cost that accompanies it. Instead, it is cost effective to abbreviate each step in the testing of parts [25] so that the test time is reduced for each part. While the steps themselves cannot be eliminated due to the coverage they provide, reduction of time in each step is the best resort. Since every step usually provides some incremental coverage, reduction of time in each step is usually resorted to than eliminating a step itself.

Reducing the cost of production test has been a topic of intense research in analog testing [25]. There are three approaches to reduce test time: i) optimal ordering of the tests, where the most failed tests are strategically placed first in order to reduce the total test time [24][5] , ii) selecting the subset of the tests to achieve the same coverage [22][13] , iii) automated development of better and more efficient tests that provide more coverage [21][29][20][27][28] and, iv) reducing the communication time by compressing tests on-chip [9][17]. To the best of our knowledge, no previous work in analog domain has addressed the problem of reducing *each individual test's time.*

Test compression for analog and mixed signal circuit is a challenging problem. Analog circuits are nonlinear systems and work with continuous signals. Compressing continuous inputs is very complex and an instance of functional optimization. Compressing tests while maintaining the same precision and recall specification is challenging. Compressing analog tests may increase the rate of false positives and results in unnecessary losses. Therefore test compression algorithm should guarantee functional equivalency and ensure the circuit will behave identically under the original and compressed tests. Test compression methods often require extra circuitry, both on-chip and off-chip to minimize communication time and compressing the tests. The additional circuitry increases the cost of the testing. Finally, optimizing RF tests are still an open challenge because compressing RF tests in time inherently destroys frequency properties of the initial test.

To reduce test time, we introduce an automated test compression methodology for analog and mixed signal circuits. We apply our test compression algorithm to stress

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