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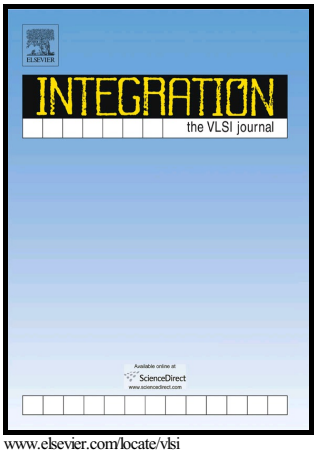

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Low-loss active inductor with independently adjustable self-resonance frequency and quality factor parameters

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Abstract_ This work presents a new low-loss active inductor whose self-resonance frequency and quality factor parameters can be adjusted independently from each other. In order to achieve this property, a new input topology has been employed which consists of cascode structure with a diode connected transistor. Furthermore, the proposed input topology makes the device robust in terms of its performance over variation in process, voltage and temperature. Additionally, RC feedback is used to cancel series-loss resistance of the active inductor, which allows self-resonant enhancement as well. Schematic and post-layout simulation results show the theoretical validity of the design. To validate the design feasibility for process, voltage and temperature changes, Monte Carlo and temperature analysis are done. Suggested structure shows inductor behavior in the frequency range of 0.3-11.3 GHz. Maximum quality factor is obtained as high as 2.1k at 5.9 GHz. Total power consumption is as low as 1mW with 1.8 V power supply.

Keywords: Active inductor, CMOS, quality factor, self-resonance frequency, low-loss

1. Introduction:

Inductors are inevitable parts of the electronic circuits especially in variety of communication and information processing applications. On the other hand, CMOS has been dominant technology to implement Integrated Circuit (IC) for almost three decades. Therefore, designers have tried to integrate inductors with this technology.

Since spiral inductors, implemented by CMOS, suffer considerably from both ohmic loss in metal and substrate loss due to the conductive silicon, so they typically exhibits the lowest quality factor. Another drawback of inductors on silicon is their excessive area coverage [1-3]. The limitations of standard CMOS spiral inductors have led researchers to consider a variety of alternatives such as Active Inductors (AIs) [4, 5]. Although plagued by higher noise and higher power consumption than their passive counterparts, AIs are theoretically capable of producing relatively high and tunable quality factors and inductance [6, 7].

Various analog architectures are suggested to emulate the electrical characteristics of inductor in literature [4-8]. However, the most famous topology which is used in designing AIs especially for high frequency applications, is Gyrator-C (GC) [9, 10]. Its popularity relies on the fact that gyrators transconductance can be adjusted with applied bias, thereby allowing for AIs whose value can be tuned electrically [9-11].

Designers do their best to improve Self-Resonance Frequency (SRF) and Quality Factor (QF), two main characteristics in term of AI performance [5]. In GC topologies, the input transistors play critical role in active inductor characterization. By selecting the input transistor's gate-source parasitic capacitance sufficiently small, then the SRF Range (SRFR) of AI improves but its QF and stability degrade. On the other hand, large input transistor guarantees the stability of AI and improves the inductance value and QF but decreases the SRFR [6]. Thus, there is a trade-off between SRF and QF.

Another main challenge for AIs designers is their ohmic loss which affect the QF. For decreasing this parasitic components many tricks are used such as Multi-Regulated Cascade stages [9, 10] or cross-coupled structures i.e. Negative Resistance (NR) [12-14]. But these methods are limited input swing and increased input referred noise. Also they need biasing transistors which makes the device larger.