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A mechanism for detecting on-chip radio frequency interference of field-programmable gate array

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ABSTRACT

One-chip measurements without modifying the physical structure of packaged integrated circuits such as field-programmable gate arrays (FPGA) is challenging. This paper proposes a sensor for detecting the radio frequency interference (RFI) on the supply inside the FPGA chip. The core of the sensor is a ring oscillator built with FPGA look-up tables. The paper proposes a model to predict the response of the ring oscillator to power supply RFI, and shows that the normalized frequency shift of the ring oscillator resulting from the interference is determined by the amplitude of the interference. This relationship is independent of the interference frequency and the size of the ring oscillator. To verify the model, simulations on transistor-level look-up tables of 130-nm and 40-nm technologies were performed. The simulation results matched well with the model. In addition to simulation, an FPGA test board was fabricated. Measurements of FPGA RFI response were performed and the results were consistent with the theoretical model. The effect of the interference on the ring oscillator provided a mechanism to detect the amplitude of the supply interference on the FPGA chip. The frequency of the ring oscillator was monitored through the supply pin by measuring the spectrum of the supply noise. The properties of the sensor, such as constant response in a wide frequency range, insensitiveness to the oscillator size, ease of implementation, and minimal modification requirement of the physical structure, made it suitable for performing on-chip FPGA measurements.

1. Introduction

Radio frequency interference (RFI) from external sources may propagate along printed circuit board traces and package wires to the chip of integrated circuits (IC). Modern ICs have complex packages. The RFI amplitude on a chip differs quite a lot from its amplitude on the pins of an IC; measuring the arrival RFI on the chip is quite challenging.

Several on-chip signal measurement methods have been reported since the 1990s. High-resolution time-domain waveforms of noise have been obtained with sampling-based techniques [1–9], and the authors of [10,11] measured the probability distribution function of power noise; however, those techniques required synchronization to a reference clock and do not fit the measurement of unpredictable external RFI.

Authors of [12] did not measure the waveform; instead, they detected the events of a considerable voltage drop in the supply. The method employed an on-chip controller and a digital interface to complete the detection. The authors of [13] provided a method to measure the two-dimensional map of supply noise; however, a controller with switches existed in the measurement circuit. The authors of [14–18] presented techniques to detect the RFI on a chip. The methods of [14–16] required a complex analog circuit, a processor core, and software to detect the RFI. The authors of [17,18] used an individual supply system for the sensor that required additional power pins; inserting sensors in a host chip considerably modifies the physical structure of a chip. The authors of [19] built an on-chip glitch detector by feeding a clock signal and its delay version to a flip-flop; however, it might be difficult to detect the glitches if there were both positive and negative ones within one clock period.

The field-programmable gate array (FPGA) is a critical IC used in a large number of electronic systems. Majority of these systems operate in RFI-intensive environments. Therefore, the RFI behavior of FPGAs is interesting for both the academic society and industry. The physical structure of an FPGA is fixed, and the chip is well packaged. Inserting external sensors into the chip is not practical. Moreover, inserting a sensor changes the physical structure of an FPGA and introduces errors in measurement results. To measure the on-field RFI on an FPGA chip

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requires a noninvasive method.

This paper introduces a method to measure the amplitude of the sinusoidal interference on the power distribution network (PDN) of an FPGA chip. A ring oscillator (RO) formed by look-up tables (LUTs) drives input/outputs (I/O) and forms the on-chip RFI sensor. The feedback signal of the sensor is the supply noise excited by the sensor and was measured at the power pin of the FPGA. In the frequency domain, the supply noise is located at the operation frequency and the harmonics of the RO. When RFI is present on the on-chip PDN, the operational frequency shifts and offers a means of monitoring the on-chip RFI. Using this method, the FPGA structure is untouched as no extra circuit needs to be inserted.

In Section 2, we provide the theoretical basis for the response of the RO to the supply RFI showing how the operation frequency of the RO is shifted by the RFI. The relationship between the shift value and the RFI amplitude is the key to the on-chip RFI measurement. Section 3 constructs a transistor-level model of an RO formed by LUTs and describes the performed HSPICE simulations. In Section 4, an FPGA test board is fabricated, and measurements are conducted. Section 5 provides a discussion, and Section 6 concludes the paper.

2. Theory

An RO comprises an odd number of inverters. Suppose that the inverter propagation delay is τ_{INV} and that the RO has N_{INV} inverters, then the operational frequency of the RO, f_{RO}, is given by (1). Referring to (2), the delay is a function of the supply voltage V_{DD}, and the function is called the static response of the inverter delay. Here, V_{DD} in (2) is a static voltage.

$$f_{RO} = \frac{1}{2N_{INV}\tau_{INV}} \tag{1}$$

$$\tau_{INV} = f_{static}(V_{DD}) \tag{2}$$

The scheme that this study follows is illustrated in Fig. 1. A single-tone RFI from external sources is applied to the RO power supply. The waveform of the supply voltage is given by (3). V_0 is the nominal voltage, A_{RFI} is the arrival RFI amplitude, and f_{RFI} is the RFI frequency.

$$V_{DD} = V_0 + A_{RFI}\sin(2\pi f_{RFI} t) \tag{3}$$

The delay of a single inverter is in the range of 0.01–0.1 ns. The RFI cycle time below 1 GHz is much larger than the inverter delay. During the switching of an inverter, its supply voltage can be considered as constant. The number of the switched inverters within one RFI cycle can be approximated with (4).

$$N_{swc} = \int_0^{T_{RFI}} \frac{dt}{f_{static}(V_0 + A_{RFI}\sin(2\pi f_{RFI} t))} \tag{4}$$

Using variable substitution, (4) can be simplified as (5.1) and (5.2).

$$N_{swc} = \frac{F(A_{RFI})}{2\pi f_{RFI}} \tag{5.1}$$

$$F(A_{RFI}) = \int_0^{2\pi} \frac{d\theta}{f_{static}[V_0 + A_{RFI}\sin(\theta)]} \tag{5.2}$$

The operational frequency of the RO under RFI is then

$$f_{RO\_RFI} = \frac{N_{swc}}{2N_{INV}} = \frac{1}{2N_{INV}} \frac{F(A_{RFI})}{2\pi f_{RFI}} \tag{6}$$

The normalized frequency shift of an RO owing to the RFI on the supply is defined by (7), where Δf_{RO_RFI} is the frequency shift caused by the RFI.

$$\frac{\Delta f_{RO\_RFI}}{f_{RO\_0}} = \frac{f_{RO\_RFI} - f_{RO\_0}}{f_{RO\_0}} \tag{7}$$

With (6) and (7), a formula for calculating the normalized frequency shift can be established and is given in (8).

$$\frac{\Delta f_{RO\_RFI}}{f_{RO\_0}} = \frac{F(A_{RFI}) - F(0)}{F(0)} \tag{8}$$

Examining (5) and (8), it can be observed that the normalized frequency shift is determined by the RFI amplitude and the static response of the inverter delay and is independent of the RFI frequency. If (8) is true, then the RFI amplitude can be evaluated by measuring the normalized frequency and performing the following conversion in (9).

$$A_{RFI} = F^{-1}\left[\left(1 + \frac{\Delta f_{RO\_RFI}}{f_{RO\_0}}\right)F(0)\right] \tag{9}$$

The above deduction does not specify the technology of the inverter. The theoretical model should apply to inverters made of LUTs in the FPGA. The following sections check the validation of the model through both simulation and measurement.

3. Simulation

To verify that the LUT-based RO follows (8), a transistor-level RO model was built and simulated in HSPICE.

As shown in Fig. 2, a 4-input LUT (4-LUT) was built out of SRAM bits and four levels of multiplexers. Each SRAM bit held a reconfigurable value, and the multiplexers were used to select the configured value. The transistor netlist of the 4-LUT was obtained by manually converting the logic units in Fig. 2 into transistor circuits.

The structure of the simulated circuit is shown in Fig. 3. An RO was built by cascading a number of 4-LUTs. The innermost select port A was used as the LUT-based inverter's input to make the propagation path as long as possible and thus provide more propagation delay information. The ROs were powered by the V_0 supply voltage. When we simulated the RFI response of the ROs, an RFI source was added to the supply.

Four types of LUT-based ROs were built as test devices; their parameters are given in Table 1. The BSIM models from SMIC 40-nm and 130-nm CMOS technologies were used as the simulation transistor models.

The first simulation studied the static response of the LUT-based inverter delay. The supply voltage V_{DD} swept statically around V_0. The inverter delay was calculated by measuring the RO cycle time. For 130-nm technology, the simulated static response of the inverter delay is shown in Fig. 4(a). Since all LUT-based inverters had the same inverter

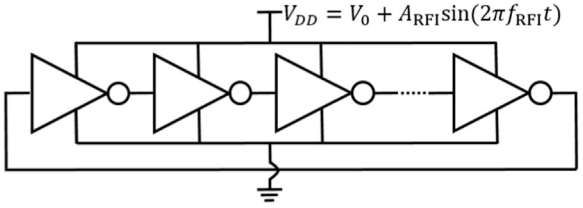

Fig. 1. RO with external RFI on supply.

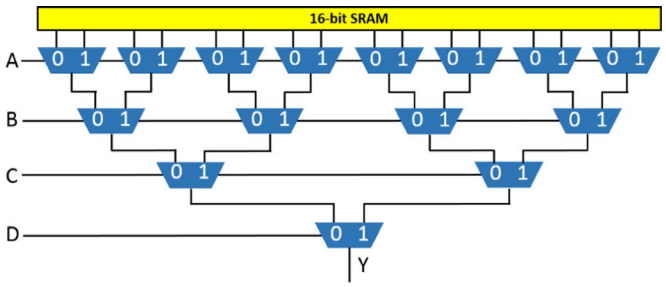

Fig. 2. Logical diagram of SRAM-based 4-LUT.