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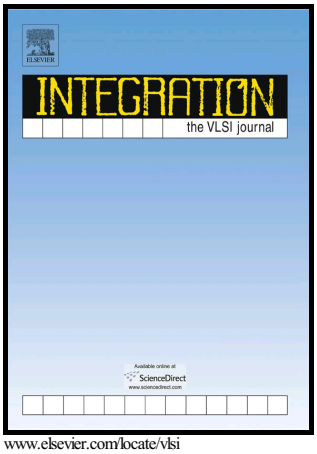

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A Fast Temperature-aware Fixed-outline Floorplanning Framework Using Convex Optimization

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Abstract

With aggressive scaling of CMOS technology, it is essential to consider chip temperature in all design levels of digital systems to improve chip reliability and leakage power consumption. In this paper, we present a two phase fixed-outline floorplanning framework that attempts to reduce the peak-temperature of the chip. The first phase distributes evenly the available dead space between the floorplan blocks of a chip, so as to reduce the peak-temperature. The second phase employs a two-stage convex optimization formulation to perform fixed-outline floorplanning such that minimizes the peak-temperature while satisfying physical constraints. To mitigate the time and computational complexity of capturing the temperature behavior, we present a less computational expensive analogous formulation that approximates the temperature of a block by its corresponding power density. Although, the corresponding power density formulation exhibits lower complexity the experimental results demonstrate its high degree of accuracy. Moreover, this formulation manages to achieve significant improvements in terms of peak-temperature and runtime for almost all of the test cases. We investigate the trade-off between peak-temperature and area as well and provide conditions that result in a reasonable reduction of peak-temperature with minimum increase of the dead space.

Keywords: Floorplanning Framework, Convex Optimization, Temperature, Fixed-outline, Power Density.

1. INTRODUCTION

Technology scaling enables designers to integrate more transistors into a single chip to achieve high performance. Aggressive scaling may lead to higher power density and temperature, which causes a localized high temperature region known as thermal hot spots. Thermal hot spots have adversarial effects on chip operation such as:
1) Decreasing reliability: Failure scenarios such as Electromigration and Hot Career Injection increase by growing thermal hot spots [1]. According to [2], a change of operating temperature by $10-15^oC$ results in a $2X$ reduction in the lifespan of devices.
2) Increasing power consumption: Temperature induces a positive feedback with leakage power consumption. This leakage may account for up to 60% of the total energy consumption in deep sub-micron technologies [3].
Consequently, the temperature has become an issue of paramount value due to its direct or indirect role in power consumption, reliability, and cooling costs. Thus it is required to consider temperature effects in all phases of digital system design.

Typical floorplanning techniques attempt to decrease wire length to improve performance and reduce energy consumption. However, as power density becomes more severe, floorplanning techniques require considering temperature as well as other typical design metrics such as area and wiring length. Maximizing the distance of two hot blocks to prevent thermal conduction is the basis of thermal aware floorplanning. The importance of the temperature-aware floorplanning is shown in [4]. Subject to the magnitude of temperature threshold the amount of performance loss by the Dynamic Temperature Management (DTM) techniques varies from 6% to 21%. This performance loss decreases to less than 2% when the temperature is considered in the floorplan stage of the chip besides to other traditional metrics. In other words, well-designed floorplans can significantly reduce the performance loss, compared to the techniques that concentrate only on DTM techniques [5].

There have been many studies on temperature-aware floorplanning and most of them do not consider a fixed-outline for the chip. These works are based on evolutionary algorithms such as Simulated Annealing (SA) [4, 6] and Genetic Algorithm (GA) [7, 8]. Healy et al. [9] have proposed a floorplanning algorithm that employs Linear Programming(LP) and SA algorithm. Their floorplanning technique consists of two phases. The first phase specifies width and height of the blocks of chip and places them within the chip using the LP algorithm. After accomplishing the LP-based floorplanning and as the second phase a SA-based refinement is carried out. Although the SA and GA algorithm are well suited for floorplanning problems, they hold a long running time and suffer scalability [5]. Most of mentioned studies resort to thermal simulator to calculate the temperature-dependent part of the floor-