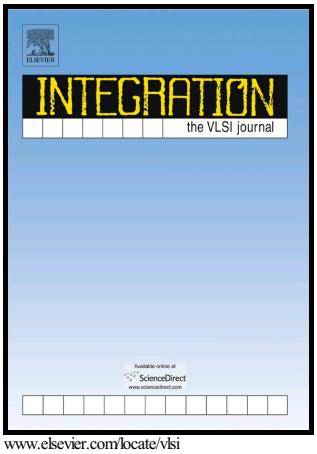


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# New Advances of High-Level Synthesis for Efficient and Reliable Hardware Design

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**Abstract**

The spectacular CMOS technology scaling will continue to evolve and dominate the semiconductor industry. This will lead to tens of billions of transistors integrated on a single chip by the year 2020. However, one significant problem is that the design productivity for complex designs has been lagging behind. In addition to several proposed techniques for dealing with the widening productivity gap, e.g., IP reuse and integration, virtual platform modeling, formal verification and others, high-level synthesis (HLS) has been touted as an important solution as it can significantly reduce the number of man hours required for a design by raising the level of design abstraction. However, existing HLS solutions have limitations, and studies show that the design quality of HLS can be inferior compared to that of manual RTL design. In this paper, we will present a set of new techniques developed recently to drastically improve HLS solutions, which not only improve the traditional design metrics such as circuit performance and energy efficiency but also emerging metrics such as circuit reliability and robustness. We will also discuss how HLS can collaborate with other techniques to provide a holistic design methodology that can enable the delivery of high-quality designs with much less design cost and much faster time-to-market.

*Keywords:* High-Level Synthesis, Designer Productivity, Quality of Results, Reliability, Security, Verification, Validation, Time to Market, Modeling, Performance, Low Power, Area Cost, Polyhedral Optimization, Parallel Languages, Interconnect Optimization, Variation Aware, Multicycle Path, IP Integration, Benchmarks

## 1. Introduction

As Dennard scaling slows down, hardware designers are under pressure to deliver:

**Area Efficiency:** For mass produced ASIC designs, silicon area is the dominant design/manufacturing cycle cost. Thus area efficiency is the key to lowering the cost of a chip. For FPGA designs used in datacenters, FPGA resource usage determines how many and what size FPGAs need to be provisioned.

**Energy efficiency:** With mobile devices, energy efficiency is critical for good battery life. At the datacenter scale, energy efficiency determines the maximum density at which devices can be packed before heat dissipation becomes a problem.

**Performance:** As more intelligence is packed into devices, the demand for performance in demanding image and video processing tasks continues to increase. Meeting or failing to meet latency and throughput targets is the difference between a good and bad end user experience.

**Complex SoCs:** The need for energy efficiency with increased performance despite the slowdown in Dennard scaling has resulted in an explosion in design complexity. In many cases, hardware designers are forced to design custom hardware to meet difficult area/energy/performance targets. In other cases, designers are creating multiple customized CPU cores, GPUs, and custom memory hierarchies.

Hardware designers also have to deal with a plethora of problems as enumerated in Table 1, including:

**Bugs:** Bugs are the bane of a hardware designer's existence. Electrical bugs in fabricated designs such as timing errors and cross-talk are very hard to isolate. Designers also inevitably create and trip over logic bugs they introduce on their own in their complex designs.

**Reliability problems:** With submicron scaling, numerous reliability issues ranging from transistor wear-out to soft errors to electromigration have gotten worse, making delivering reliable hardware more difficult than ever. Designing hardware with unreliable components that sometimes generate the wrong results becomes increasingly difficult as more and more components become vulnerable to these problems.

**Security threats:** The above reliability threats can be thought of as *unintelligent* adversaries as each can be modeled to predict its behavior. Security threats are *intelligent*, *malicious*, and much more difficult to model. Furthermore, not only can an intelligent adversary cause a chip to fail, but the adversary can also cause it to leak sensitive information. For the software community, this problem is real as multiple high-profile cases of vulnerabilities and successful attacks have made the news. As the complexity of hardware design increases and more and more personal items become connected in the Internet of Things, making them potential valuable targets for attackers, designers will need to start thinking about hardware security as well.