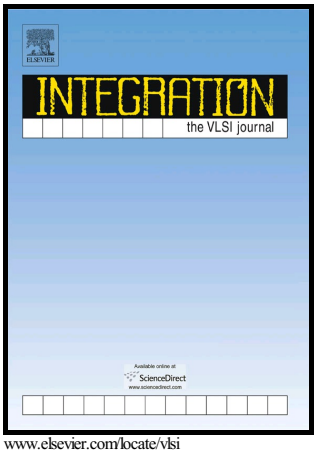

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Contemporary CMOS Aging Mitigation Techniques: Survey, Taxonomy, and Methods

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Abstract

The proposed paper addresses the overarching reliability issue of transistor aging in nanometer-scaled circuits. Specifically, a comprehensive survey and taxonomy of techniques used to model, monitor and mitigate Bias Temperature Instability (BTI) effects in logic circuits are presented. The challenges and overheads of these techniques are covered through the course of this paper. Important metrics of area overhead, power and energy overhead, performance overhead, and lifetime extension are discussed. Furthermore, the techniques are assessed with regards to ease of implementation and the ability to cope with challenges such as increase in manufacturing induced process variations. Finally, a taxonomy of the surveyed techniques is presented to facilitate generalization of the discussed approaches and to foster new inspiring techniques for this important reliability phenomenon leading to advancements in the design of defect-tolerant digital circuits.

Keywords: NBTI, PBTI, HCI, aging prediction model, aging monitoring, aging adaptation and mitigation

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