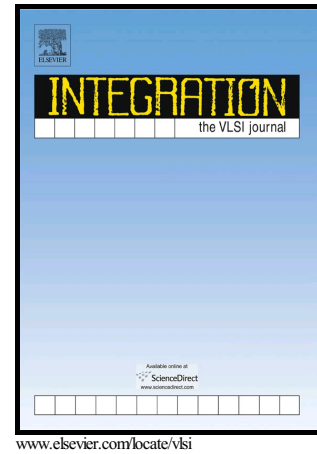


Author's Accepted Manuscript

Contemporary CMOS Aging Mitigation
Techniques: Survey, Taxonomy, and Methods

Navid Khoshavi, Rizwan A. Ashraf, Ronald F.
DeMara, Saman Kiamehr, Fabian Oboril, Mehdi B.
Tahoori



PII: S0167-9260(17)30187-6
DOI: <http://dx.doi.org/10.1016/j.vlsi.2017.03.013>
Reference: VLSI1325

To appear in: *Integration, the VLSI Journal*

Received date: 5 September 2016
Revised date: 9 February 2017
Accepted date: 24 March 2017

Cite this article as: Navid Khoshavi, Rizwan A. Ashraf, Ronald F. DeMara, Saman Kiamehr, Fabian Oboril and Mehdi B. Tahoori, Contemporary CMOS Aging Mitigation Techniques: Survey, Taxonomy, and Methods, *Integration, the VLSI Journal*, <http://dx.doi.org/10.1016/j.vlsi.2017.03.013>

This is a PDF file of an unedited manuscript that has been accepted for publication. As a service to our customers we are providing this early version of the manuscript. The manuscript will undergo copyediting, typesetting, and review of the resulting galley proof before it is published in its final citable form. Please note that during the production process errors may be discovered which could affect the content, and all legal disclaimers that apply to the journal pertain.

Contemporary CMOS Aging Mitigation Techniques: Survey, Taxonomy, and Methods

Navid Khoshavi^a, Rizwan A. Ashraf^b, Ronald F. DeMara^a, Saman Kiamehr^c,
Fabian Oboril^c, Mehdi B. Tahoori^c

^a*Department of Electrical and Computer Engineering, University of Central Florida (UCF)*

^b*Oak Ridge National Laboratory, Oak Ridge, TN, 37830*

^c*Department of Computer Science, Karlsruhe Institute of Technology (KIT)*

Abstract

The proposed paper addresses the overarching reliability issue of transistor aging in nanometer-scaled circuits. Specifically, a comprehensive survey and taxonomy of techniques used to model, monitor and mitigate Bias Temperature Instability (BTI) effects in logic circuits are presented. The challenges and overheads of these techniques are covered through the course of this paper. Important metrics of area overhead, power and energy overhead, performance overhead, and lifetime extension are discussed. Furthermore, the techniques are assessed with regards to ease of implementation and the ability to cope with challenges such as increase in manufacturing induced process variations. Finally, a taxonomy of the surveyed techniques is presented to facilitate generalization of the discussed approaches and to foster new inspiring techniques for this important reliability phenomenon leading to advancements in the design of defect-tolerant digital circuits.

Keywords: NBTI, PBTI, HCI, aging prediction model, aging monitoring, aging adaptation and mitigation

Email addresses: navid.khoshavi@ucf.edu (Navid Khoshavi), ashrafra@ornl.gov (Rizwan A. Ashraf), ronald.demara@ucf.edu (Ronald F. DeMara), kiamehr@kit.edu (Saman Kiamehr), fabian.oboril@kit.edu (Fabian Oboril), mehdi.tahoori@kit.edu (Mehdi B. Tahoori)

Download English Version:

<https://daneshyari.com/en/article/4970682>

Download Persian Version:

<https://daneshyari.com/article/4970682>

[Daneshyari.com](https://daneshyari.com)