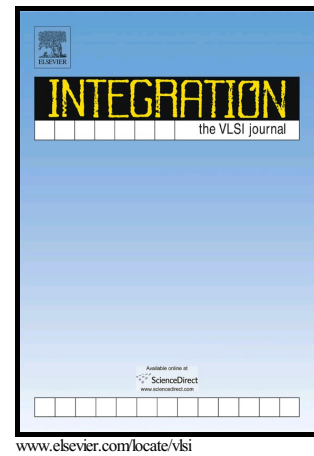


# Author's Accepted Manuscript

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PII: S0167-9260(17)30320-6  
DOI: <http://dx.doi.org/10.1016/j.vlsi.2017.05.006>  
Reference: VLSI1338

To appear in: *Integration, the VLSI Journal*

Received date: 4 October 2016  
Revised date: 24 March 2017  
Accepted date: 20 May 2017

Cite this article as: Simone Acciarito, Alessandro Cristini, Gianluca Susi, Gaurav Mani Khanal, Gian Carlo Cardarilli, Luca Di Nunzio, Rocco Fazzolari and Marco Re, Hardware design of *LIF with Latency* neuron model with memristive STDP synapses, *Integration, the VLSI Journal*, <http://dx.doi.org/10.1016/j.vlsi.2017.05.006>

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# Hardware design of *LIF with Latency* neuron model with memristive STDP synapses

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## Abstract

In this paper, the hardware implementation of a neuromorphic system is presented. This system is composed of a Leaky Integrate-and-Fire with Latency (LIFL) neuron and a Spike-Timing Dependent Plasticity (STDP) synapse. LIFL neuron model allows to encode more information than the common Integrate-and-Fire models, typically considered for neuromorphic implementations. In our system LIFL neuron is implemented using CMOS circuits while memristor is used for the implementation of the STDP synapse. A description of the entire circuit is provided. Finally, the capabilities of the proposed architecture have been evaluated by simulating a motif composed of three neurons and two synapses. The simulation results confirm the validity of the proposed system and its suitability for the design of more complex spiking neural networks.

*Keywords:* *Leaky Integrate-and-Fire with Latency (LIFL), Neuron, Synapse, STDP, Memristor, Neuromorphic System, analog VLSI.*

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## 1. Introduction

In recent years, many efforts have been done in order to reproduce the brain behaviour; this is due to a remarkable capacity of the brain itself to process data

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