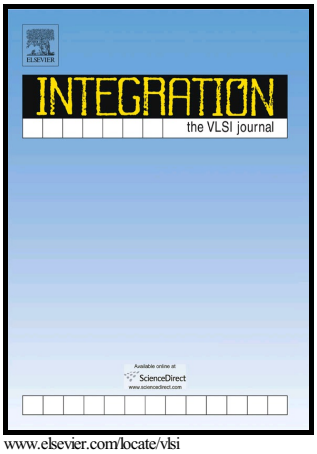
Author's Accepted Manuscript

On Advance towards Sub-Sampling Technique in Phase Locked Loops-A Review

Anu Tonk, Neelofer Afzal



www.elsevier.com/locate/vlsi

PII: S0167-9260(17)30354-1
DOI: http://dx.doi.org/10.1016/j.vlsi.2017.06.004
Reference: VLSI1344

To appear in: *Integration, the VLSI Journal*

Received date: 28 March 2016
Revised date: 29 May 2017
Accepted date: 5 June 2017

Cite this article as: Anu Tonk and Neelofer Afzal, On Advance towards Sub-Sampling Technique in Phase Locked Loops-A Review, *Integration, the VLSI Journal,* http://dx.doi.org/10.1016/j.vlsi.2017.06.004

This is a PDF file of an unedited manuscript that has been accepted fo publication. As a service to our customers we are providing this early version o the manuscript. The manuscript will undergo copyediting, typesetting, an review of the resulting galley proof before it is published in its final citable form Please note that during the production process errors may be discovered whic could affect the content, and all legal disclaimers that apply to the journal pertain

ACCEPTED MANUSCRIPT

On Advance towards Sub-Sampling Technique in Phase Locked Loops-A Review

Anu Tonk[1], Neelofer Afzal

Department of ECE, F/o Engineering & Technology, Jamia Millia Islamia, New Delhi, India.

tonkanu.saroha@gmail.com

neelofer.afzal@yahoo.com

Accepted manuscript

ABSTRACT

This paper presents a symmetric review of academic and accomplished research endeavors in the field of Sub-Sampling Phase Locked Loop (SSPLL) design. Adequate emphasis has been given to understand the yearn for development of Sub-Sampling PLLs. Techniques that have emerged over the recent few years in context of better FOM, Jitter and Phase Noise reduction while maintaining extraordinary circuit performance in Sub-Sampling PLLs with CMOS/VLSI technology, have been captured in this paper. Consecutively, the main inspiration of this study is to present an overview of the PLL fundamentals, furtherance from analog to Digital PLL and various noises encountered in the different PLL components, important for the reader to have a better understanding about the design and analysis of Sub-Sampling PLLs.

Keywords:

Analog PLL, Digital Phase Locked Loop (DPLL), Dead-zone, VCO, frequency divider, Sub-Sampling PLL, Integer-N, SSPD, Figure of Merit (FOM), Fractional-N

1. INTRODUCTIONA wide use of Phase locking schemes has originated in the field of power systems: for selective harmonic detection system [1], Grid connected power electronic equipments [2]; Instrumentation systems: for mode-locked laser sustaining high stable dual frequency laser and radio distribution [3]; for Optical links: in developing clock synthesizer for overcoming bandwidth limitations of copper medium communication above tens of Gb/s [4]. Impulse radio Ultra wide band (UWB) CMOS circuits have also been developed for short reach transmission, early breast cancer detection systems, confocal visualization of a cancer target [6]-[7]. There has been progressive improvement in the performance of Analog Phase-Locked Loops with operating frequencies extending to 8GHz and beyond. On the other hand Digital PLLs, have turn up as an option in certain applications like Bluetooth, Zig-bee applications [16], cellular transmitters, 4G [17]-[18], etc. Besides the obvious advantages, digital version of PLL alleviates a number of problems associated with its analog counterpart, namely: Sensitivity to dc drift and component saturation, difficulty in building higher order loops, bulky loop filter components, need for initial calibration [8],[15]. DPLLs can work at very low frequency also; support faster locking speed unlike Analog PLLs which have slow and unreliable self acquisition [19]. ADPLLs [16] offer benefits of smaller area, capability of wide self-calibrations, programmability and trouble-free portability. Further, deep–submicron CMOS has been driving the technology towards implementing most of the PLL building blocks in digital form [13]-[14], most of them being hybrid these days. A high-speed hybrid clock recovery circuit has been described in [20],[23] for disk drive applications; A new hybrid PLL frequency

[1] Tel.: +91-8447488082

Download English Version:

https://daneshyari.com/en/article/4970690

Download Persian Version:

https://daneshyari.com/article/4970690

Daneshyari.com