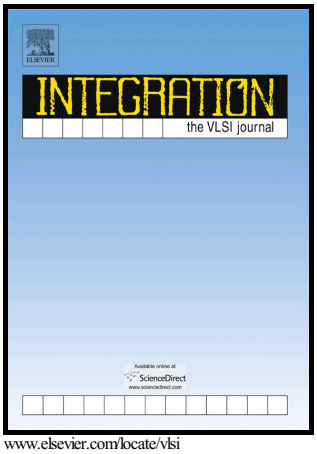

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Exploiting Bounds Optimization for the Semi-formal Verification of Analog Circuits

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***Abstract*—This paper proposes a semi-formal methodology for modeling and verification of analog circuits behavioral properties using multivariate optimization techniques. Analog circuit differential models are automatically extracted and their qualitative behavior is computed for interval-valued parameters, inputs and initial conditions. The method has the advantage of guaranteeing the rough enclosure of any possible dynamical behavior of analog circuits. The circuit behavioral properties are then verified on the generated transient response bounds. Experimental results show that the resulting state variable envelopes can be effectively employed for a sound verification of analog circuit properties, in an acceptable run-time.**

***Index Terms*—Analog Circuits; Global Optimization; Verification; Qualitative Simulation**

I. Introduction

Process parameters and input fluctuations have an adverse impact on analog circuits functionality and robustness [1]. Moreover, analog circuits responses are very sensitive to the uncertainty in the initial values of their continuous state variables. Indeed, different initial conditions may create totally dissimilar dynamic behaviors. Therefore, verification techniques ensuring that a circuit model satisfies its desired behavior with the inclusion of parameters, input and initial condition variability are of great importance. However, the verification of analog circuits is time-consuming and requires a great deal of expertise on the part of the designer. The difficulty mainly arises from the knowledge-intensive nature of analog circuits and their infinite state and parameters space [2].

SPICE [3] is the state-of-the-art in terms of accurate analog circuit simulation. It includes Monte Carlo (MC) statistical simulation capabilities which analyze a model multiple times with a random change of model parameters. MC analysis can be employed to characterize the circuit dynamic under the effect of process variation and estimates its yield rate [1]. However, it is very difficult to show a specific behavior through simulation, if we are not provided with a complete knowledge of the circuit parameters and inputs. Furthermore, MC-based methods cannot guarantee an exhaustive coverage of the circuit state space [4]. This lack of observability may have a disastrous effect when the aim of the simulation is to verify whether the circuit will go through critical operating conditions [5]. A large number of simulations can be required to achieve acceptable accuracy at a prohibitively high computational cost and memory resources. Moreover, circuit simulator-based verification involves the use of device parameter variation for a particular process at the transistor level, making the verification process unmanageable at lower level of abstraction. Besides, the user has only access to the numerical simulation results and cannot extract the mathematical model of the circuit which is usually hard coded.

Based on rigorous mathematics, formal verification is the most promising verification method in terms of exhaustiveness and completeness [6]. However, due to the complexity of analog circuits devices models, formal verification techniques are very hard to apply without resorting to over-simplified circuit models in the verification process. Their use has been mainly limited by their computational overhead and lack of automation [2].

This paper tries to address some of the above shortcoming and challenges. Mainly, the objectives can be summarized as follow: (1) the development of a homogeneous environment for the modeling and practical verification of analog circuits; (2) the computation of a complete characterization of the circuit behavior under multiple type of uncertainties; and (3) the sound verification of analog circuit behavioral properties within a reasonable computation time.

Qualitative simulation is a semi formal technique introduced by Bonarini and Bootempi [7] to complement numerical simulations and predict the behavior of incompletely known and fuzzy systems [8]. Based on global optimization, it generates an over-approximated envelope of a dynamical system trajectories modeled as Fuzzy differential equations. Furthermore, the computed bound can be considered as a complete description of the uncertain dynamical model, as it contains almost any possible behavior of the circuit. Therefore, qualitative simulation can be a potential choice for the characterization of analog circuit behavior in time domain.

In this paper, we propose an environment for modeling and verification of analog circuits behavioral properties. First, we automatically generate device-level analog circuit augmented differential equations from their netlist, which take into account the uncertainty in their parameters, inputs and initial conditions. After that, we compute envelopes of their transient behavior using a modified qualitative simulation algorithm. That is, we extended the qualitative simulation method to take into consideration not only the uncertainty in the initial values of the state variables but also the variation of the circuit parameters and inputs. We also provide the necessary steps to formulate the core optimization problem for better convergence and faster simulations. Our method generates effective over-approximations of the state space reached starting from a continuous region of initial condition. Finally, we automatically verify whether the circuit model satisfies a specified functional properties. Our verification environment is powerful in handling properties connected to: the dynamic