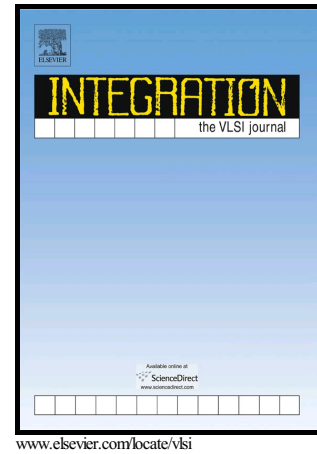


# Author's Accepted Manuscript

## A New Hybrid Algorithm for Analog ICs Optimization based on the Shrinking Circles Technique

Maryam Dehbashian, Mohammad Maymandi-Nejad



PII: S0167-9260(16)30071-2  
DOI: <http://dx.doi.org/10.1016/j.vlsi.2016.09.009>  
Reference: VLSI1246

To appear in: *Integration, the VLSI Journal*

Received date: 27 April 2016  
Revised date: 19 August 2016  
Accepted date: 26 September 2016

Cite this article as: Maryam Dehbashian and Mohammad Maymandi-Nejad, / New Hybrid Algorithm for Analog ICs Optimization based on the Shrinking Circles Technique, *Integration, the VLSI Journal*, <http://dx.doi.org/10.1016/j.vlsi.2016.09.009>

This is a PDF file of an unedited manuscript that has been accepted for publication. As a service to our customers we are providing this early version of the manuscript. The manuscript will undergo copyediting, typesetting, and review of the resulting galley proof before it is published in its final citable form. Please note that during the production process errors may be discovered which could affect the content, and all legal disclaimers that apply to the journal pertain.

# A New Hybrid Algorithm for Analog ICs Optimization based on the Shrinking Circles Technique

Maryam Dehbashian<sup>a</sup>, Mohammad Maymandi-Nejad<sup>a,1</sup>

<sup>a</sup> *Department of Electrical Engineering, Ferdowsi University of Mashhad, Mashhad, Iran*

## Abstract

This paper presents a novel technique named the Shrinking Circles to enhance the performance of optimization algorithms embedded in automated sizing tools of analog ICs. This technique creates a balance between the exploration and exploitation capabilities when the optimization algorithm is converging to a possible optimum point. With the help of the shrinking circles concept, we upgrade a hybridization version of Gravitational Search Algorithm with Particle Swarm Optimization (Advanced GSA\_PSO). Accordingly, a developed tool for the automation of analog ICs sizing is proposed. The performance of this tool is evaluated by two cases: minimizing the power consumption of a two-stage CMOS op-amp and simultaneous minimizing the circuit area and power consumption of a folded-cascode op-amp. In this paper, the corners analysis is also incorporated into the proposed circuit sizing tool based on a straightforward procedure by which this tool not only can obtain the solutions being robust against process, voltage, and temperature (PVT) variations, but also it alleviates the computational burden. Comparisons with available methods show that the proposed tool performs much better in terms of efficiency.

## Keywords

Analog ICs optimization, Automated sizing tool, The shrinking circles, Advanced gravitational search algorithm and particle swarm optimization (Advanced GSA\_PSO), Corners analysis.

## 1. INTRODUCTION

Although the analog block occupies a small area of the entire integrated circuit, it is one of the key parts of ICs and its optimal design is certainly as important as the digital block's design. The implementation and integration of analog, digital and RF circuits are provided through VLSI technology on the same chip and with the same technology as a complete system-on-a-chip. Therefore, in this way the latest analog circuits would be supplied to the industry. But the main problem is that the robust and optimal design of an analog circuit is a challenging process which involves complicating trade-offs between design objectives, parameters and constraints. The manual design of analog circuits is very complex, costly, and time consuming as well as requiring highly skilled designers [1]. For this reason, researchers have been investigating methods in the analog circuit design automation since more than thirty years ago [2], and their achievements have been presented as Electronic Design Automation (EDA) tools [3].

The analog circuit design procedure consists of topology selection, circuit sizing, and layout synthesis. This paper concentrates on the circuit sizing due to its significant importance with assumption that the circuit topology is already selected by the designer.

The analog ICs sizing tools include two main sections, i.e., *synthesis* and *optimization* which are linked together. *Synthesis section* creates a sized circuit by taking into account two important input factors, i.e., the desired specifications and topology of the circuit [4]. Synthesis approaches used in the analog ICs sizing tools can be classified into *knowledge-based* and *optimization-based* categories. In the knowledge-based approach, a pre-designed plan is separately created for each circuit topology based on designer experience and design equations. In contrast, the optimization-based approach applies an optimization process instead of a design plan to size the circuit components. This process is an iterative procedure in which design variables are updated at each iteration until a stop criterion is satisfied.

The optimization-based approach includes an iterative loop, an optimization engine together with an evaluation engine. The evaluation engine is typically implemented using one of the three following approaches: an equation-based optimization, a simulation-based optimization, or a modeling-based optimization approach [5]. Synthesis approaches used in analog ICs sizing tools are classified and illustrated in Fig. 1. This figure gives a general overview of advantages and disadvantages of the synthesis approaches, indicating that the simulation-based optimization approach has more advantages in comparison with above-mentioned approaches. The only deficiency of this approach is its relatively long computation time compared to other

<sup>1</sup>Corresponding author.

E-mail addresses: maymandi@um.ac.ir (M. Maymandi-Nejad).

Download English Version:

<https://daneshyari.com/en/article/4970742>

Download Persian Version:

<https://daneshyari.com/article/4970742>

[Daneshyari.com](https://daneshyari.com)