
# Improvement of etching and cleaning methods for integration of raised source and drain in FD-SOI technologies

M. Labrot, F. Cheynis, D. Barge, P. Maury, M. Juhel, S. Lagrasta, P. Müller

PII: S0167-9317(17)30136-3
DOI: doi: 10.1016/j.mee.2017.04.009
Reference: MEE 10514

To appear in: *Microelectronic Engineering*

Received date: 20 March 2017
Revised date: 6 April 2017
Accepted date: 11 April 2017

Please cite this article as: M. Labrot, F. Cheynis, D. Barge, P. Maury, M. Juhel, S. Lagrasta, P. Müller , Improvement of etching and cleaning methods for integration of raised source and drain in FD-SOI technologies. The address for the corresponding author was captured as affiliation for all authors. Please check if appropriate. Mee(2017), doi: 10.1016/j.mee.2017.04.009

# IMPROVEMENT OF ETCHING AND CLEANING METHODS FOR INTEGRATION OF RAISED SOURCE AND DRAIN IN FD-SOI TECHNOLOGIES

**M. Labrot[a,b], F.Cheynis[b], D.Barge[a], P.Maury[a], M.Juhel[a], S.Lagrasta[a], P.Müller[b]**

*[a]STMicroelectronics, 850 rue Jean Monnet, F-38926 Crolles Cedex, France.*
*[b]Aix Marseille Université, CNRS, CINaM UMR 7325, Case 913 campus de Luminy, 13288 Marseille cedex France.*

**Abstract**

The Fully-Depleted Silicon-on-Insulator (FD-SOI) technology for advanced CMOS devices is based on SOI substrates formed by an ultra-thin Si or SiGe film on a thick insulator. A reduction of parasitic resistances of such CMOS components is obtained with the Raised Source and Drain (RSD) technology. In this work we show that modifying the Siconi™ plasma-based etching process widely used in microelectronic and/or combining it to wet-etching methods allows to improve the principal steps of fabrication of RSD FD-SOI CMOS devices.
More precisely, using sampling areas on 300 mm wafers that simulate the principal stages of FD-SOI building, (i) we show that a modified SiCoNi process may be used to increase the etching selectivity necessary to dissolve the oxide layer while maintaining a low-k spacer of high quality, (ii) we propose a combination of optimized SiCoNi-dry and wet etching that reduces the post-etching roughness and the contamination level of the channel surface before the subsequent epitaxy.

*Keywords:* SiBCN, SiGe, SiCoNi™ Preclean, FD-SOI, Raised Source/Drain, WET clean

## 1. Introduction

The scaling of CMOS devices down to nanometric sizes has lead to various integrations strategies to control short channel effects. Two distinct integrations are now clearly identified for technological nodes below 20 nm: FINFET integration [1, 2] and FD-SOI [3].

FDSOI integration requires the use of very thin channel materials, typically below 7 nm to obtain an accurate control of the channel [4, 5]. Such dimensions are inadequate for junction engineering in the source and drains, which thus needs to be raised by Epitaxy. This technique is commonly referred to as Raised Source Drain (RSD) in the literature [6].

Figure 1 schematizes the principal fabrication steps of RSD devices. The basic brick for designing and building a FDSOI-based device consists in a SOI substrate formed by an ultra-thin Si or SiGe film, defining the device channel, on a thick insulator (BOX for buried oxide) bonded to a Si substrate. In the first steps of the process, the SOI substrate is topped by a 3D gate insulated from the channel by a High-K dielectric layer ($HfO_2$). The whole surface is covered with thin low–k dielectric layers (0p) of silicon nitride (typically $Si_3N_4$ or SiBCN). This step is followed by a photoresist coating which, after photolithography, exposes denuded zones for further etching of the low-k dielectric layers (step 2). The etching leaves resist residues that are removed by successive dry (plasma) and wet strips but leads to the formation of an oxide layer (step 3). The step 4 consists in removing the so-formed oxide layer (while avoiding any silicon nitride