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Assessing the forming temperature role on amorphous and polycrystalline HfO_2-based 4kbit RRAM arrays performance

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Abstract

The impact of temperature during the forming operation on the electrical cells performance and the post-programming stability were evaluated in amorphous and polycrystalline HfO_2-based arrays. Forming (between -40 and 150 ºC), reset and set (at room temperature) operations were applied using the incremental step pulse with verify algorithm (ISPVA). The improvements achieved on the forming operation in terms of time and voltages reduction do not impact the subsequent reset/set results. ISPVA perturbations in LRS/HRS current distributions are almost negligible after the first reset/set operation. In this study the best improvement in forming operation in terms of yield, voltage values and cell-to-cell variability is achieved in polycrystalline samples at 80 ºC.

Keywords

RRAM, 4kbit-array, amorphous HfO_2, polycrystalline HfO_2, temperature impact, forming

1. Introduction

Resistive Random Access Memories (RRAM) based on HfO_2 is one of the most promising technology candidates for replacing Flash memories [1]. This technology has shown high-integration density, fast low-power switching operations [2], and compatibility with CMOS processes [3]. The choice of a proper Metal-Insulator-Metal (MIM) technology for RRAM cells, exhibiting good uniformity and low switching voltages, is still a key issue for array structures fabrication and reliable electrical operation. Such a process step is mandatory to bring this technology to a maturity level.

The RRAM switching behavior is based on the electrical modification of the conductance of a MIM stack: the set operation moves the cell into a Low Resistance State (LRS), whereas reset operation brings the cell back to a High Resistance State (HRS) [4]. In order to activate the resistive switching behavior, the RRAM cells require a preliminary forming operation [3]. This initial operation plays a fundamental role in determining the subsequent devices performance [5].

In this work, the forming operation was performed at different temperatures on 4kbits arrays in order to study their impact on switching voltages, LRS/HRS current distributions and on the post programming stability.

2. Experimental

In order to ensure a reliable accuracy for statistical calculations the measurements were performed on on-wafer 4kbits memory arrays (Fig. 1(a)). One complete 4kbits array was characterized at each forming temperature. The 1T-1R RRAM device is constituted by a select NMOS transistor and a resistor manufactured in 0.25 µm BiCMOS technology. The transistor also sets the current compliance. Its drain is in series to a variable resistor connected to the bitline (BL). The variable resistor is a MIM device integrated on the metal line 2 of the CMOS process. The cross-sectional TEM image of the integrated RRAM cell is shown in Fig. 1(b). The MIM resistor is a $TiN/HfO_2/Ti/TiN$ stack of 150 nm TiN layers deposited by magnetron sputtering, a 7 nm Ti layer (under TiN top electrode), and an 8 nm HfO_2 layer grown by Atomic Vapor Deposition (AVD) process at low and high temperature resulting either in amorphous (A-array) and polycrystalline (P-array) HfO_2 films, respectively. The resistor area is equal to 0.4 μm^2.

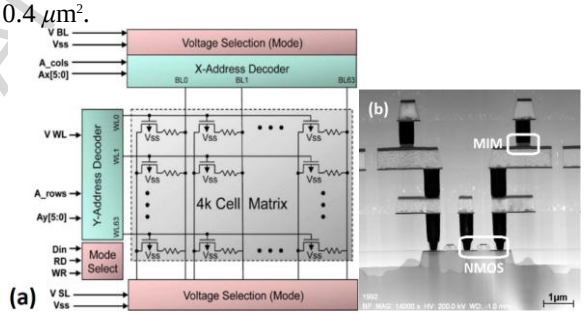

Fig.1: Block diagram of the 4kbit memory array (a) and cross-sectional TEM image of the 1T-1R integrated cell (b).

The electrical characteristics were obtained by means of a set-up based on the RIFLE SE test system working together with the Cascade PA200 semi-automatic probe system. In order to control the formation and rupture of the conductive filament (CF), the Incremental Step Pulse with Verify Algorithm (ISPVA) [6] is applied instead of a simple DC voltage sweep [7]. The ISPVA technique consists of a sequence of increasing voltage pulses (Fig. 2) on the BL during set and forming operations, whereas this sequence is applied on the source line (SL) during reset operation: t_{pulse} = 10 µs, $t_{fall/rise}$ = 1 µs. The amplitude of the pulses in reset and set operations ranges between V_{pulse} = 0.2−3 V increasing with 0.1 V, whereas in forming ranges between V_{pulse} = 2−5 V increasing with 0.01 V. The applied transistor gate voltage values through the wordline (WL) were 2.7 V for reset and 1.4 V for set and forming. After every pulse a Read-verify operation is performed with V_{WL} = 1.4 V, V_{read} = 0.2 V (applied over the BL) for 10 µs. When the Read current reaches the target value of 18 µA the set and forming operations are stopped,