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Research paper

1/*f* and RTS noise in InGaAs nanowire MOSFETs

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ABSTRACT

Low-frequency noise measurements were performed on high-performance InGaAs nanowire MOSFETs. 1/f noise measurements show number fluctuations, rather than mobility fluctuations, as the dominant noise source. The minimum equivalent input gate voltage noise reported here is 80 $\mu m^2 \mu V^2/Hz$, among the lowest values for III-V FETs, and showing the feasibility of a high-quality, low trap density, high-k gate oxide on InGaAs.

1. Introduction

Due to their high electron mobility, III-V materials, such as InGaAs, are attractive as a channel material in high-performance field-effect transistors (FETs). Utilizing nanowires (NWs) as the channel in such devices offers improved electrostatic control and enables the use of highly scaled gate lengths [1]. However, the trap density in III-V FETs with a foreign high-k oxide is typically high (compared with Si/SiO_2 devices), which can degrade the transistor performance and reliability significantly [2]. Thus, accurate and reliable measurements of the interface and oxide quality of III-V FETs are required for the device characterization and the process optimization. Conventional oxide characterization methods, such as C-V and charge pumping methods, cannot be used for ultra small devices without a body contact. Instead, low-frequency (LF) noise measurements can be utilized to analyze the performance and reliability of highly scaled devices [3].

In this paper, we present a low-frequency (LF) noise study (1/*f* as well as RTS noise) on high-performance InGaAs NW MOSFETs [4]. 1/*f* noise measurements show number fluctuations, rather than mobility fluctuations, as the dominant noise source. Furthermore, a low minimum equivalent input gate voltage noise of 80 μm^2 $\mu V^2/Hz$ is achieved, showing the feasibility of a high-quality gate oxide on InGaAs.

2. Device fabrication

The $In_{0.85}Ga_{0.15}As$ NWs are formed on semi-insulating InP:Fe by selective area MOCVD growth using HSQ as a growth mask [5]. Each device consists of a single nanowire. Highly doped ($N_D \sim 5 \cdot 10^{19}$ cm^{-3}) InGaAs source/drain contacts are formed in a second growth step using an HSQ dummy gate (Fig. 1(a)). Ti/Pd/Au source/drain metal is deposited by thermal evaporation. After surface precleaning by Ozone, $(NH_4)_2S$ (10%) for 20 min, and five cycles of in situ TMA1 pulses, Al_2O_3/HfO_2 (5/45 cycles, EOT ≈ 1.2 nm) is deposited as the gate oxide by ALD at 300/100 °C. Ni/Pd/Au gate metallization by thermal evaporation completes the process. A schematic of a fabricated device is depicted in Fig. 1(b). Details on the device fabrication can be found in [6].

3. Methods and results

Excellent DC performance was reported for these devices previously, with a peak transconductance of 2.9 mS/μm, a minimum subthreshold slope of 77 mV/decade and an on-current of 565 μA/μm (at I_{off} = 100 nA/μm), all at V_{ds} = 0.5 V, the highest reported on-current for any transistor [6]. Furthermore, it was shown that these transistors operate in the quasi-ballistic regime with a transmission of about 70%, which was obtained from quantized conductance measurements at 10 K, and was shown to be valid also at room temperature [5].

Here, we performed 1/*f* and RTS noise measurements on devices with varying gate lengths (L_g = 50–85 nm) and gate widths (W = 27–100 nm). W refers to the gated perimeter of the nanowire.

For both types of measurements, a Lake Shore Cryotronics CRX-4 K probe station was used to contact the transistors and to control the temperature. When performing the 1/*f* noise measurements, a low-noise current preamplifier (model SR570 from Stanford Research Systems) was utilized to supply a constant drain voltage of 50 mV and to amplify the drain current signal. The output of the current preamplifier was connected to a lock-in amplifier (model SR830 from Stanford Research

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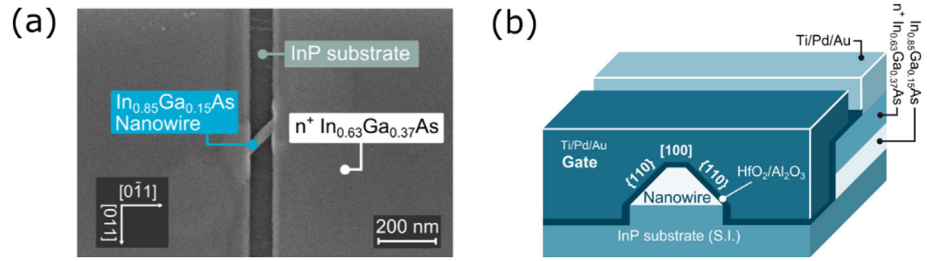

Fig. 1. (a) SEM image (top view) after the nanowire growth. (b) Schematic figure of a fabricated device.

Systems) to measure the drain current noise (S_{Id}). A Keysight B2912A source measure unit (SMU) was used to set the gate voltages and to monitor the source current during the measurements.

For the RTS noise measurements, only the Keysight B2912A SMU was utilized to set the drain and gate voltages and to measure the drain current.

The $1/f$ noise measurements show that the normalized drain current noise (S_{Id}/I_d^2) is inversely proportional to the gate area $A = L_g W$ (at a fixed drain current), indicating that the LF noise originates from the channel rather than from the source/drain resistance (Fig. 2(a)). If the LF noise had arisen from the source/drain resistance instead, S_{Id}/I_d^2 would have been independent of A.

In contrast to a previous study on highly scaled InGaAs GAA MOSFETs [3], our measurements show that number fluctuations (rather than mobility fluctuations) are the dominant LF noise source, as the normalized drain current noise follows g_m^2/I_d^2 (instead of $1/I_d$) in all our devices. This observation is exemplified in Fig. 2(b) for a single transistor with $L_g = 50$ nm and $W = 27$ nm, but is valid for all transistors (independent of L_g and W) and is here reported for quasi-ballistic devices.

As shown in Fig. 2(c), we observe low values for the equivalent input gate voltage noise ($S_{VG} = S_{Id}/g_m^2$) over a large gate voltage overdrive ($V_{ov} = V_{gs} - V_T$) range with a minimum value of 80 μm² μV²/Hz, demonstrating an excellent oxide quality in our devices. Assuming elastic tunneling of electrons to and from the trap states, the corresponding trap density can be calculated by using [7]

$$N_t = \frac{fWL_G C_{ox}^2 S_{VG}}{q^2 k_B T \lambda}. \quad (1)$$

In Eq. (1), C_{ox} is the oxide capacitance per unit area and λ is the tunneling attenuation length in the gate oxide, given by $\lambda = \left(\frac{4\pi}{h}\sqrt{2m^*\Phi_B}\right)^{-1}$ [7]. Assuming an effective electron mass of $m^* = 0.23\ m_e$ [8] in Al_2O_3 and an oxide barrier height of $\Phi_B = 2.4$ eV [9], the trap density is as low as

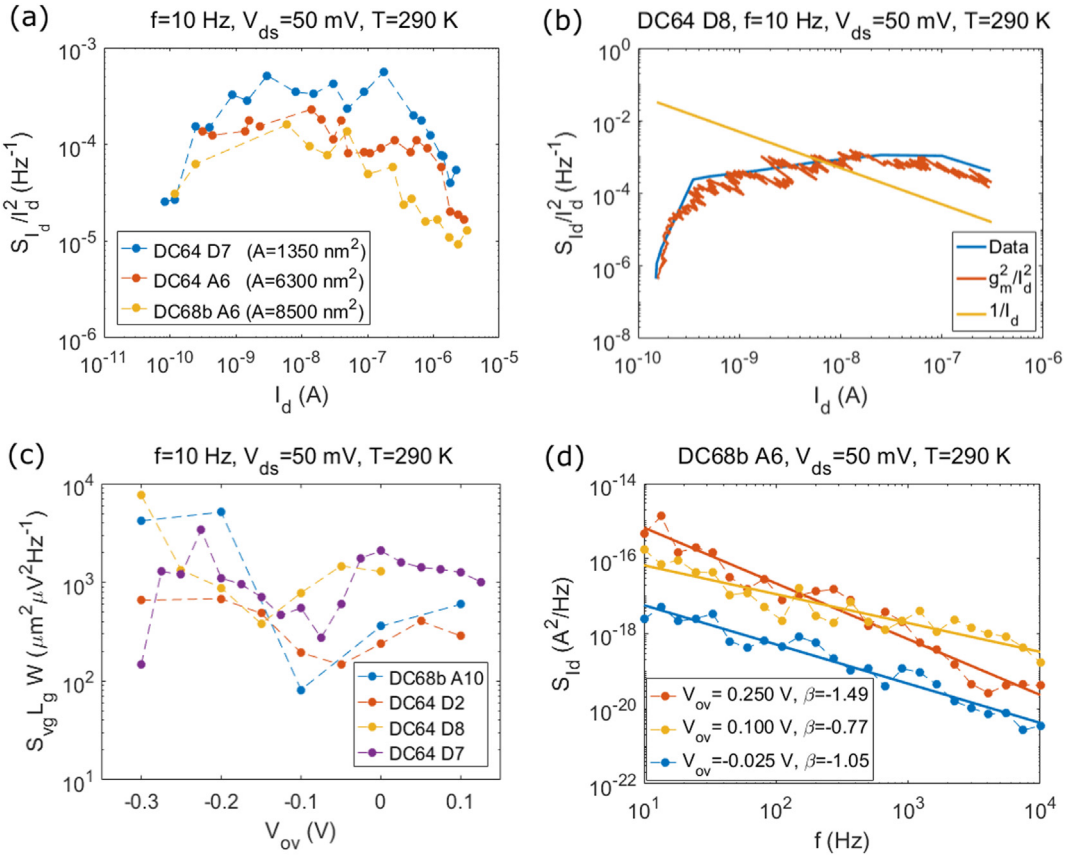

Fig. 2. (a) Impact of the gate area scaling on the normalized drain current noise, showing that the LF noise originates from the channel. (b) The normalized drain current noise follows the transconductance in all devices, indicating that number fluctuations are the dominant noise mechanism. (c) Low values for the equivalent input gate voltage noise over a large gate voltage overdrive range for device DC68b A10 ($L_g = 70$ nm, $W = 78$ nm), DC64 D2 ($L_g = 50$ nm, $W = 27$ nm), DC64 D8 ($L_g = 50$ nm, $W = 27$ nm) and DC64 D7 ($L_g = 50$ nm, $W = 27$ nm). (d) Gate voltage dependence on the f^{β} noise exponent (β) for transistor DC68b A6 ($L_g = 85$ nm, $W = 100$ nm).