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Efficient methodology to extract interface traps parameters for TCAD simulations

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ABSTRACT

In this work, a methodology to estimate ATLAS TCAD simulation parameters from experimental data is presented, with the aim of analyzing the impact of interface traps in the MOSFET threshold voltage variability of a particular technology. The method allows to calculate the parameters that define the trap behavior in TCAD simulations (trapped charge, trap energy level and capture cross section) from the parameters that can be experimentally measured (capture and emission times and single-trap threshold voltage shift). The availability of these simulation parameters will allow to study RTN and/or BTI-related variability through TCAD simulations, in reasonable computing times.

1. Introduction

To improve the performance of integrated circuits, the size of devices has been progressively reduced and, currently, the nanometer range has been reached. As a consequence, the discreteness of charge is reflected in the electrical performance of devices, leading to device variability [1–3]. For instance, charge trapping/detrapping in/from interface states can be observed in the form of Random Telegraph Noise (RTN) and/or Bias Temperature Instabilities (BTI), which introduce random and/or permanent shifts in the threshold voltage [4,5]. Therefore, understanding the physics behind this variability and how it impacts the device behavior is essential to introduce suitable countermeasures into the fabrication processes, device architecture and/or circuit design.

TCAD simulations can be a fast and adequate approach to evaluate, from experimental data, the statistical impact of interface traps (ITs) on the threshold voltage shift (ΔV_{th}) of MOSFETs of a particular technology [6]. It must be taken into account, however, that the parameters that describe the IT behavior in these simulators, i.e. energy level (E_{trap}), cross section (σ_{trap}) and trapped charge (Q_{trap}) differ from those that can be experimentally obtained, such as capture (τ_c) and emission (τ_e) times and single-trap induced threshold voltage shift ($\Delta V_{th}(IT)$), so that the simulation-experiment link is not straightforward. In this work, a procedure to translate the empiric trap parameters (τ_c, τ_e and $\Delta V_{th}(IT)$) into the main TCAD physical parameters (E_{trap}, σ_{trap} and Q_{trap}) is proposed.

It will be shown that Q_{trap} can be estimated from static simulation data, whereas the relation between (E_{trap}, σ_{trap}) and (τ_c, τ_e) can be evaluated from transient data, considering a suitable compact model. The proposed methodology will allow RTN and BTI variability studies using TCAD simulations.

2. Device structure and simulation methodology

2.1. Device structure

A bulk nMOSFET structure was defined in ATLAS TCAD tool (from Silvaco) and calibrated using experimental I_D-V_G curves measured in transistors (W/L = 300 nm/300 nm). Fig. 1 shows the adopted flow diagram for device calibration procedure. First, since simulation time in 2D is shorter than in 3D, 2D devices were simulated using the nominal device parameters and a Gaussian doping profile. The error between the simulated and one representative measured I_D-V_G curve was minimized by varying doping and other technological parameters (as the EOT or underlapping length).

When the 2D calibration was finished, that is, when the error was less than a given value set by the user (1% in this work), the final 2D fitting parameters were used as initial parameters in 3D simulations, where the same algorithm was repeated. This procedure reduces the computation time (hours) because most of the simulations were performed in 2D. Fig. 2a shows the net doping profile and some dimensions of the device obtained after the calibration. Fig. 2b shows the final simulated (red line) and measured (black squares) I_D-V_G curves in linear and logarithmic scale; the good agreement validates the calibration procedure.

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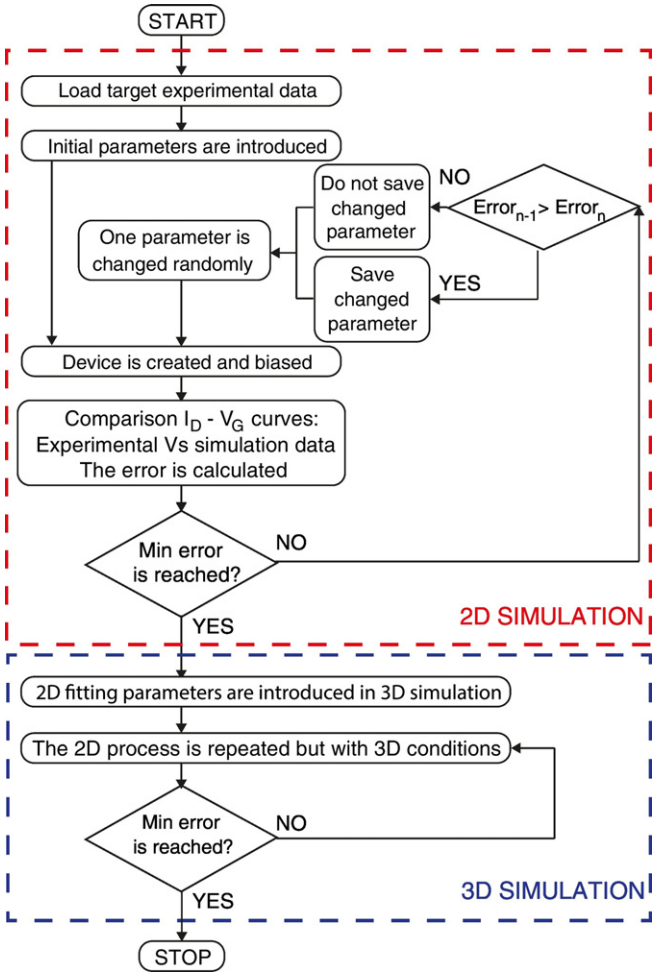

Fig. 1. Flow diagram of the TCAD device calibration procedure.

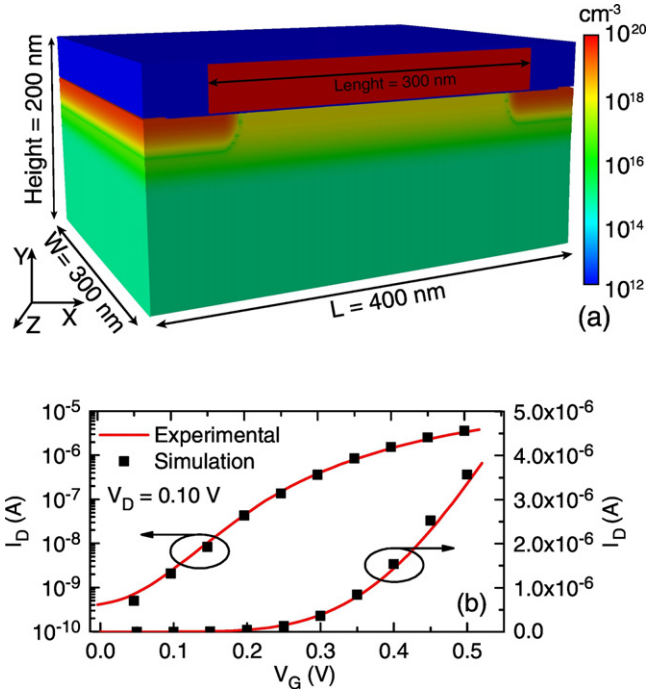

Fig. 2. MOSFET structure showing the channel doping (a). Experimental (black squares) and simulated (red lines) I_D-V_G curves of the device (b). The nominal Vth of the device was 0.37 V and the estimated EOT was 1.5 nm. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

2.2. Simulation methodology

The I_D-V_G characteristics in Fig. 2b were considered as reference and the effect of additional discrete traps located at the semiconductor/oxide interface on the device threshold voltage (V_{th}) was analyzed. To improve the simulation accuracy, around the IT location the mesh was refined (steps of 1 nm). Multiple traps (N_{trap}) were expected in the device interface, which were characterized by their E_{trap}, σ_{trap} and Q_{trap}, and whose spatial distribution and number change from device to device. Traps in the oxide bulk were not taken into account in this work because their effect could be estimated using the presented approach by simply considering interface traps with different trapped charge. Moreover, other sources of variability as Random Dopant Fluctuations (RDF) or Line Edge Roughness (LER), whose effects could be combined with those of ITs [3], although not negligible in real devices, in this work have not been considered, in order to analyze exclusively the shifts in the threshold voltage, ΔV_{th}, related to ITs. However, although not considered, it should be emphasized that: first, RDF and/or LER would only affect the parameter Q_{trap} of our methodology (not those parameters related to the dynamic simulations) and, second, the RDF effect on V_{th} variability could be included in the proposed methodology since RDF, as fixed traps, could be somehow equivalent to the ITs introduced in the oxide, affecting the Q_{trap} parameter. Regarding LER, further characterization and analysis should be considered to include this variability source in the simulation procedure.

To understand the impact of each analyzed parameter (E_{trap}, σ_{trap} and Q_{trap}), simulations where two parameters were kept constant while one was changed were performed.

3. Static simulations

In this section, 3D-static simulations were performed to evaluate the effect of the traps spatial distribution and the value of Q_{trap} on the device threshold-voltage shift (ΔV_{th}), when changes in σ_{trap} and E_{trap} were neglected. In this case, the ITs in the device were considered to be charged with a charge equal to Q_{trap} (so, these simulations are equivalent to consider that there is a charge Q_{trap} at the position of the IT). Device V_{th} was calculated from the simulated I_D-V_G curves using the constant current method, for a threshold current $I_{th} = 1$ μA, when $V_D = 0.10$ V was applied.

3.1. Spatial distribution of traps

The contribution to the device ΔV_{th} of each individual trap, ΔV_{th}(IT), was analyzed. Fig. 3a shows a simulated current density map at the oxide/semiconductor interface for one device with $N_{trap} = 12$ and $Q_{trap} = e^-$ (arbitrarily chosen). Numbers indicate the order in which the traps were introduced in the simulated device. As it can be observed, the current density decreases near the ITs, which can be explained because the traps create a barrier that can hinder the electron transport [7], leading to a change of V_{th}. Fig. 3b shows how each trap in Fig. 3a individually impacts the device V_{th}, by introducing a change ΔV_{th}(IT). Note that ΔV_{th}(IT) varies from trap to trap. As already demonstrated in [2,7], the trap impact on V_{th} depends on its position within the channel: traps in the channel (i.e. 1, 2, 4, 6, 7, 11) cause larger ΔV_{th}(IT) than traps closer to the source/drain contacts (i.e. 3, 5, 8, 9, 10).

To analyze in more detail this behavior, Fig. 4 shows the impact of one IT on V_{th} (IT) when it was swept along the z-axis (width) (Fig. 2a) and x-axis (length) (Fig. 2b). As it can be observed, the trap impact on V_{th} does not depend on the position along the z-axis (width). On the other hand, ΔV_{th}(IT) depends on the trap location along x-axis, dramatically decreasing when traps were close to the source/drain diffusions.