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Single-Trap Analysis of Hot-Carrier-Induced Gate Oxide Degradation in Flash Memory Cells

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***Abstract*—Using a test structure containing two memory cells with a shared floating gate (FG), we analyzed the processes of hot-electron-induced charge trapping in the FG oxide with a single-trap resolution. Unlike the traditional RTN-based method for single-trap study, the proposed approach allows one to detect not only the interface traps showing capture-emission events in the time domain, but also to resolve virtually all individual trapping-detrapping events in the floating gate oxide during the program-erase cycling.**

Keywords: flash memory, SuperFlash, non-volatile memory, floating gate, hot electron, oxide degradation, charge trapping, single electron.

1. Introduction

As the MOSFET technology is scaled down, the effect of individual charges in the gate oxide on the modulation of transistor characteristics (threshold voltage V_t or drain read current I_d) becomes more pronounced. The analysis of single trap behavior by means of sophisticated electrical characterization methods has led to a deeper understanding of the physical nature of the traps and the associated mechanisms, such as hot-electron degradation, random telegraph noise, BTI, etc [1].

According to a simple 1-D electrostatics, a V_t shift (ΔV_t), induced by a single trap at the gate oxide-substrate surface, is inversely proportional to the gate oxide capacitance. In case of the floating gate (FG) memory cell,

$$\Delta V_t = \frac{q t_{ox}}{CR \cdot \varepsilon_{ox} S}, \tag{1}$$

where t_{ox} and S are the FG oxide thickness and area, respectively, and CR is the control gate-to-FG capacitive coupling coefficient (coupling ratio).

Since the FG oxide thickness typically is not scaled much below 80-90 Å due to data retention requirements, and because $CR<1$, floating gate cells demonstrate much larger single-trap modulations of threshold voltage compared to regular MOSFETs of the same technology node. Single surface-trap capture-emission-related V_t instabilities, showing up as random telegraph noise (RTN), present a serious concern for scaled multilevel FG memories, and thus has drawn considerable attention from the nonvolatile memory community. Giant RTN signals with amplitudes much higher than predicted by (1) have also been reported, together with a number of theories explaining this phenomenon [2-3].

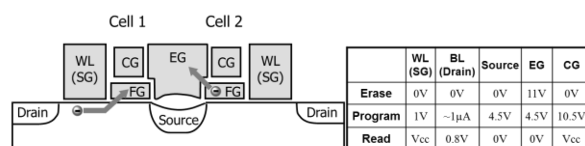
The number of individual traps contributing to RTN, and the single-trap-related RTN amplitude is traditionally analyzed by sampling cell V_t or read current in the time domain. At the same time the time domain sampling reveals only a fraction of the cycling-induced electron traps which are located close to the oxide-substrate interface, and can be easily charged and discharged. The large portion of the traps does not show up as a random telegraph signal, and remains filled by electrons. These traps however may eventually release electrons over the device lifetime, which will result in V_t shift.

Ideally we would like to see all the traps in the FG oxide, generated and/or filled during program-erase cycling, and the amplitudes of the corresponding V_t modulations. However, the analysis of cycling-induced hot-electron degradation in regular FG cells with a single-trap accuracy is hardly possible because the effect of a single trap in the FG oxide on the cell threshold voltage (V_t) is typically much smaller compared to the variations of cell V_t between program-erase cycles, caused by statistical fluctuations of the FG charge.

Earlier we proposed a differential approach to suppress the abovementioned “erase/program noise” [4], using a test structure consisting of two cells with shared FG [5], and demonstrated that the method is sensitive enough to resolve the events of an individual electron trapping and detrapping in the FG oxide. In this paper we used the proposed method to quantify the charge trapped in the FG oxide during program-erase cycling up to 100,000 cycles, and to analyze the statistical distribution of single-trap-induced V_t modulations. We were also able to experimentally measure the reference 1-D ΔV_t value (1) for an electron trapped at the FG oxide-substrate interface.

2. Experimental

For the current study we used 3rd generation SuperFlash® cells (ESF3), see Fig. 1, manufactured using 40nm CMOS technology [6-7]. The cell utilizes tip-(corner-) enhanced Fowler-Nordheim electron tunneling for erase and source-side hot-electron injection for programming.



	WL (SG)	BL (Drain)	Source	EG	CG
Erase	0V	0V	0V	11V	0V
Program	1V	~1μA	4.5V	4.5V	10.5V
Read	Vcc	0.8V	0V	0V	Vcc

Fig. 1. The structure and typical operation conditions of ESF3 memory cell. Two mirrored cells sharing common source are shown. Electron transfer directions during programming (Cell 1) and erase (Cell 2) are schematically shown by arrows. WL is the word line (select gate), CG is the coupling gate, EG is the erase gate, BL is the bit line, SL is the source line, and FG is the floating gate.

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