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Research paper

Effects of ultra-shallow ion implantation from RF plasma onto electrical properties of 4H-SiC MIS structures with SiO_x/HfO_x and SiO_xN_y/HfO_x double-gate dielectric stacks

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ABSTRACT

This study presents the first results concerning technology and characterization of MIS structures with double-gate dielectric stacks fabricated on 4H-SiC substrates after ultra-shallow fluorine and nitrogen implantation from RF plasma. The gate stack was composed of ultra-thin (~5 nm) pedestal PECVD SiO_x or SiO_xN_y, and top (~43 nm) HfO_x fabricated by means of reactive magnetron sputtering process. The RF implantation procedure was optimized in order to obtain the maximum concentration of implanted ions very close to the SiC/dielectric interface. The electrical characterization of fabricated MIS structures have shown the improvement of electro-physical properties of MIS structures after the Post-Metallization Annealing, reduced Q_{eff}/q and D_{it} values after RF ion implantation of MIS devices compared to corresponding reference structures, as well as the increase of effective permittivity for the double-gate dielectric stack with pedestal SiO_xN_y layer. Furthermore, all examined SiC-MIS test structures fabricated after plasma implantation processes are characterized by a reduction in a leakage current density, and very significant increase of the mean breakdown voltage value.

1. Introduction

It is commonly known that high-*k* dielectric materials have already replaced thermal silicon dioxide (SiO_2) or oxynitride (SiO_xN_y) as the gate dielectric in nowadays Ultra-Large-Scale-Integration (ULSI) silicon (Si) devices. For example, the equivalent thickness of gate dielectric layers is smaller than 1 nm in the 22 nm node [1]. The change of a gate dielectric layer is also a very important issue from the point of view of silicon carbide (SiC) based devices [2]. It can be connected with the fact that in 2011, Cree Inc. has introduced commercially available Metal-Oxide-Semiconductor Field-Effect-Transistors (MOSFETs) for the first time. The main problem with SiC devices is the interface states density (D_{it}) value at SiC/SiO_2 interface, which is two order of magnitude higher than in the case of Si/SiO_2 [3]. This is due to the fact that 'classical' thermal oxidation of silicon carbide, which is more complex material from the point of view of chemical structure compared to the silicon, results in the formation of interfacial layer having several sources of impurities, such as: microcrystals [4], interstitial atoms of silicon, and carbon [5], or carbon dimers [6]. Although a continuous improvement of the SiC/SiO_2 interface quality is observed, the fabrication of an 'ideal' semiconductor/dielectric system is still a great scientific challenge.

And thus, several methods for the improvement of electro-physical properties of SiC/dielectric system are being investigated nowadays. One of the possible solutions is the application of novel gate dielectric stack. In this research area, the most visible progress, and increasing number of investigations have been observed for hafnia-based gate dielectric materials technology, characterization, and modeling, either for Si-based devices [7,8], or for SiC structures for high power, and high frequency electronics [9,10]. However, fluorine or nitrogen incorporation into SiC surface region has been also investigated as one of the possible solutions for the fabrication of SiC/dielectric stack with improved electro-physical properties [11,12]. We have recently demonstrated that ultra-shallow fluorine or nitrogen implantation from radio frequency (RF) 13.56 MHz plasma results in the improvement of several electro-physical properties of silicon/silicon dioxide, or silicon/hafnium oxide (HfO_x) systems [13,14]. Furthermore, it has been shown in the literature that ion implantation results in the decrease of threshold voltage (U_T) value instability [15], and significant enhancement of mobility of MOSFETs [16]. Dielectric layers have also been found to be more resistant to ionizing radiation [17], Fowler-Nordheim (F-N) tunneling injection stress, and channel hot electron stress. Moreover, the decrease of interface state density (D_{it}), as the most important from the MOSFET operation point

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of view, after fluorine implantation into silicon surface region was also observed [18].

In this study, we present for the first time the experimental results of the ultra-shallow RF plasma ion implantation of fluorine and nitrogen into silicon carbide subsurface area. The originality of the proposed method was that the implantation process was carried out in classical Reactive Ion Etching (RIE), and Plasma Enhanced Chemical Vapor Deposition (PECVD) reactors. In this work, the effects of plasma ion implantation onto electro-physical properties of 4H-SiC-MIS structures based on low-temperature SiO_x/HfO_x, and SiO_xN_y/HfO_x double-gate dielectric stacks will be presented and investigated.

2. Experimental

In this work, we have used 4H-SiC substrates with 5 μm thick n-type epi-layer doped to $1 \div 5 \times 10^{15}$ cm^{-3} (Cree Inc.). Prior to the fabrication of MIS capacitors SiC substrates have been cleaned by means of modified RCA method (piranha + SC1 + SC2 + BHF dipping). The first process during the fabrication of MIS structures was the backside ohmic contacts formation in order to avoid the influence of the temperature treatment onto electro-physical parameters of final gate-stack. As the back-contact the titanium (Ti) layer formed by sputtering method was used that was followed by RTP 950 °C annealing in forming gas. The ultra-shallow RF plasma ion implantation procedures have been performed by means of standard PECVD, and RIE reactors made by Oxford Instruments (System 80^+). Both implantation processes were performed at room temperature (RT) for 2 min with the flow of carbon tetrafluoride (CF_4), or ammonia (NH_3) 50 sccm to get plasma discharge in 200 mTorr with 120 W of RF power applied to the reactive chamber. Before the gate-stack fabrication, the substrates were once again cleaned by means of RCA method. The gate stack of fabricated MIS structures was composed of two gate dielectric materials, i.e., the bottom silicon oxide or oxynitride films (~5 nm) were fabricated by PECVD method (@ 350 °C), while top dielectric hafnium oxide (~43 nm) layer was deposited by means of RF reactive magnetron sputtering process at RT (PlasmaLab System 400 made by Oxford Instruments Plasma Technology). Sputtering process was also used to fabricate aluminum (Al) which was used as the top-metal gate. Split experiments with Post-Metallization Annealing (PMA) process at 300 °C, vacuum atmosphere, of final MIS structures, have been done. And thus, the MIS structures were divided into the 'reference' – without either the RF ion implantation process into the SiC substrates, or the PMA process, and structures fabricated on modified by implantation process substrates followed by PMA.

The electrical measurements were performed with the Keithley 4200 semiconductor characterization system equipped with SUSS PM-8 probe station. The MIS capacitors with the gate area of $A = 1.9 \times 10^{-3}$ cm^2 and $A = 7.1 \times 10^{-4}$ cm^2 were used allowing the determination of basic electro-physical properties of the investigated stacks. Possible changes of the electrical parameters were investigated by means of capacitance-voltage (CV), as well as current-voltage (IV) measurements, while the changes of structure and chemical composition of investigated SiC/dielectric system were studied by means of spectroscopic ellipsometry and Secondary Ion Mass Spectroscopy (SIMS), in order to get the fluorine and nitrogen distribution profiles and their concentration in the obtained silicon/dielectric system.

The distribution and concentration of fluorine and nitrogen ions in the SiC/dielectric system were analyzed using Ultra-Low-Energy (ULE) SIMS. The SIMS measurements were conducted using a SAJW-05 instrument with a Balzers quadrupole-based mass analyzer (QMA-410) [19]. The apparatus was also equipped with a 06-350E Physical Electronics Ar^+ ion gun. The samples were sputtered with Ar^+ primary ions at 1.32 keV impact energy. The use of an ultra-low energy primary beam for sputtering helped to reduce atomic mixing and to produce profiles with high depth resolution. The ion beam which was approximately 100 μm in diameter with a current of 70 nA was rastered over a 3000 μm × 3000 μm area.

Basic electro-physical parameters of obtained MIS devices have been evaluated. It has to be underline that all parameters are 'effective', i.e., estimated for the entire double-gate dielectric stack. The effective Equivalent Oxide Thickness (EOT) value of double-gate dielectric stack was determined based on the maximum value of capacitance (C_{MAX}) in the accumulation, however, the values of C_{MAX} were taken frequently directly from CV curve since resulted capacitance values were almost the same. The EOTs of investigated in this work dielectric stacks have been estimated based on the maximum capacitance of MIS structure in the accumulation regime. We have used the following equation:

$$EOT = \frac{\varepsilon_0 \cdot \varepsilon_i \cdot A}{C_{MAX}} \tag{1}$$

where C_{MAX} was obtained by using two-point method of Majkusiak and Jakubowski [20].

$$C_{MAX} = \left(\frac{C_1 + C_2}{2} + \frac{kT}{q}\left|\frac{C_2 - C_1}{U_{G2} - U_{G1}}\right|\right) + \sqrt{\left(\frac{C_1 + C_2}{2} + \frac{kT}{q}\left|\frac{C_2 - C_1}{U_{G2} - U_{G1}}\right|\right)^2 - C_1 C_2} \tag{2}$$

where A is a gate area, $kT/q = 0.0258$ V and C_1, C_2, U_{G1}, U_{G2} are coordinates of two points selected in the accumulation regime of CV characteristic of MIS structure.

Effective electric permittivity of SiO_x/HfO_x and SiO_xN_y/HfO_x double-gate dielectric stacks was calculated by using following equation:

$$\varepsilon_i = C_{MAX}\frac{t_i}{A} \tag{3}$$

where t_i is a thickness of SiO_x/HfO_x and SiO_xN_y/HfO_x measured after spectroscopic ellipsometry. For this purpose, the spectroscopic ellipsometer UVISEL made by Horiba Jobin-Yvon was used. Such an apparatus allows for measurements in the wavelength range of 190–850 nm.

For flat-band voltage value (U_{FB}) estimation we have calculated, at first, the flat-band capacitance by using the following equation:

$$C_{FB} = \frac{C_i \cdot \left(\frac{\varepsilon_s \cdot A}{\lambda}\right)}{C_i + \left(\frac{\varepsilon_s \cdot A}{\lambda}\right)} \tag{4}$$

where C_{FB} is a flat-band capacitance, C_i is an equivalent double-gate dielectric stack capacitance, ε_s is the permittivity of SiC, A is a gate area, and λ is a Debye length which is calculated, as follows:

$$\lambda = \left(\frac{\varepsilon_s \cdot kT}{q^2 \cdot N_s}\right)^{\frac{1}{2}} \tag{5}$$

where q is an electron charge, and N_s is dopant concentration. On the basis of the above evaluation, we could find the flat-band voltage value of the MIS structure directly from a particular CV characteristic.

Effective charge density of the double-gate dielectric stack was evaluated, as follows:

$$Q_{eff}/q = \frac{\varepsilon_i}{t_i} \cdot (\varphi_{MS} - U_{FB}) \tag{6}$$

where for an aluminum metal gate the work function (φ_{MS}) was assumed as:

$$\varphi_{MS} = \varphi_{Al} - \left[\varphi_{SiC} + \frac{E_g}{2} - \varphi_F\right] \cong -1.04 - \varphi_F \tag{7}$$

where φ_F is the Fermi potential.