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Research paper

Ultra-high thermal stability and extremely low D_{it} on HfO_2/*p*-GaAs(001) interface

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ABSTRACT

Molecular beam epitaxy (MBE) HfO_2 films ~1.5 nm thick were directly deposited on freshly grown GaAs(001)-4 × 6 reconstructed surfaces. The hetero-structure exhibits outstanding thermal stability up to 900 °C with excellent capacitance-voltage (*C-V*) and leakage current density-electric field (*J-E*) characteristics. We have extracted low interfacial trap densities (D_{it}'s) with minimum value of 1.3×10^{11} eV^{-1} cm^{-2} from the measured quasi-static *C-V* (*QSCV*) characteristics. The smallest frequency dispersion of the *C-Vs* for the MBE-HfO_2/*p*-GaAs(001) is ~5.2% at frequency range of 500 to 1 MHz and no trap-induced humps were observed in the *C-Vs*, as measured at 100 °C and 150 °C. Also, the leakage current density remains low of 10^{-8}(A/cm^2) at E < ± 3 (MV/cm). The key to passivate GaAs in attaining low D_{it}'s and high-temperature thermal stability is to ensure the cleanness of GaAs surface prior to the high-κ deposition.

1. Introduction

Pushing higher-speed and lower-power electronic devices requires the integration of high carrier mobility channels such as (In)GaAs to be an essential part of the ultimate CMOS circuits [1–3]. Si complementary metal-oxide-semiconductor (CMOS) since the 45 nm node has used high-κ HfO_2-based gate dielectrics in scaling-down the capacitance effective thickness (CET) [4]. It is, therefore, very important to continue to employ HfO_2 in the new technology for integration with the present platform. A perfected SiO_2/Si interface exhibits thermal stability beyond 1100 °C and extreme low interfacial trap density (D_{it}) of ~$10^{10}eV^{-1}cm^{-2}$. The high-κ and metal gate (HKMG) Si CMOS 14 nm node still employed a SiO_2 ~ 0.4 nm thick inserting between high-κ and Si as the passivation layer for tailoring interfacial property to attain a D_{it} of ~$10^{11}eV^{-1}cm^{-2}$. To fulfill the aggressive scaling of EOT < 1 nm, depositing HfO_2-based oxides directly on high mobility channels without a low-κ interfacial layer is a must for future technology. To achieve the excellent interfacial properties approaching those at the SiO_2/Si interface, perfecting the high-κ HfO_2/GaAs interfacial quality would be the main theme and a big challenge.

In fabricating GaAs inversion-channel MOS field-effect-transistors (MOSFETs) [5–8], there are two essential requirements: (I) a high-quality oxide/GaAs interface with a low D_{it} and (II) high thermal stability beyond 900 °C for sufficient source/drain dopant activation. Note that an amorphous HfO_2 layer recrystallizes at ~600 °C, and forms a monoclinic phase with four domains causing leakage paths, inadequate for the gate stack applications [9].

Several attempts on inserting interfacial passivation layers (IPLs) such as Si [10,11] and Ge [12] between HfO_2 and GaAs yielded a D_{it} < 10^{12} eV^{-1} cm^{-2} have been reported, but the thermal stability was poor with temperatures higher than 700 °C. In great contrast, atomic-layer-deposited (ALD) [13] Y_2O_3 *in-situ* directly on GaAs(001) has shown effective passivation with high temperature thermal stability to 900 °C, which enables the possibility of fabricating GaAs MOSFETs by the gate-first approaches.

In this work, amorphous HfO_2 1.5 nm thick was directly e-beam evaporated on freshly grown GaAs(001). For the first time, without any IPLs, the HfO_2/GaAs(001) interface remains intact after 900 °C rapid thermal annealing (RTA). The frequency dispersion of the capacitance-voltage (*C-V*) characteristics for MBE-HfO_2/*p*-GaAs(001) is 1.56% per decade, lowest ever achieved in HfO_2/GaAs hetero-structures. Moreover, we have extracted a low D_{it} of 1.3×10^{11} eV^{-1} cm^{-2} using the quasi-static *CV* (*QSCV*) measurement.

2. Experimental

In our multi-chamber UHV system [14], *p*-GaAs epi-layers doped with Be were grown on *p*-GaAs(001) wafers in a solid-source GaAs-

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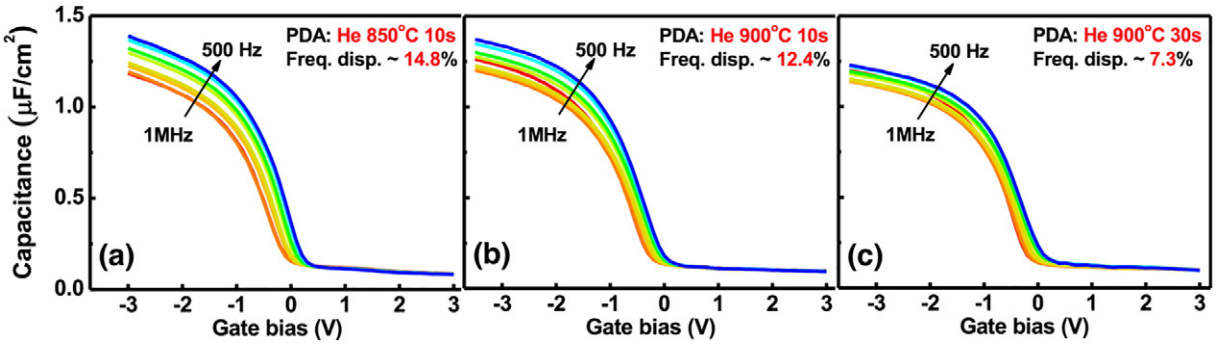

Fig. 1. The capacitance-voltage (*C-Vs*) characteristics measured from 1 MHz to 500 Hz under post deposition annealing conditions of (a) 850 °C 10s, (b) 900 °C 10s, and (c) 900 °C 30s.

based MBE chamber. The samples were then *in-situ* transferred under ~10^{-10} Torr to an As-free oxide-MBE chamber for attaining a 4 × 6 reconstructed surface by annealing the samples to ~560 °C. The substrate temperature was lowered to ~120 °C for the oxide deposition to prevent the recrystallization of HfO_2 during deposition. HfO_2 1.5 nm thick was e-beam evaporated directly onto GaAs(001), followed by of e-beam evaporated Al_2O_3 5 nm thick as a cap. We then removed the samples from the UHV system to fabricate MOS capacitors (MOSCAPs). The samples were firstly post deposition annealed (PDA) at 550 °C in N_2 ambient for 20 min to improve oxide film quality and subsequently rapid-thermal-annealed (RTA) to 850–900 °C under different durations to examine the interfacial thermal stability. Ni 100 nm thick was e-beam evaporated as circular gate electrodes through a shadow mask with a diameter of 100 μm and Ti/Au were deposited as back ohmic contact. To further improve the interfacial quality, the samples were post metallization annealed (PMA) in forming gas (H_2 15%/N_2 85%) at 400 °C for duration of 5 min. *C-V* characteristics were measured at room temperature in dark by Agilent 4284A Precision LCR meter, and J-E and QSCV characteristics were measured by using Agilent 4156C Precision Semiconductor Parameter Analyzer. Moreover, we have also performed *C-V* measurements at elevated temperatures of 100 °C and 150 °C in dark by using Agilent E4980A Precision LCR meter.

3. Results and discussion

One critical issue in attaining high-performance GaAs(001) inversion-channel MOSFETs is to reduce the S/D contact resistivity. Besides lowering the Schottky barrier height, it is essential to fully activate the implanted dopants; this means that high temperature annealing above 900 °C is required. However, in oxides/GaAs(001) hetero-structures, thermal stability above 800 °C is rarely reported, except our earlier work of $Ga_2O_3(Gd_2O_3)$ on GaAs [15] and $In_{0.2}Ga_{0.8}As$ [16]. Recently, we reported trivalent Y_2O_3 deposited by ALD and MBE on passivating GaAs(001), with both achieving high thermal stability of ~900 °C and $D_{it} < 10^{12}$ eV^{-1} cm^{-2} [17–19]. To integrate the current HfO_2-based HKMG technology on GaAs is of no less importance for the future GaAs MOSFETs. Hence, the first step is to examine the thermal stability of the MBE-HfO_2/GaAs(001) hetero-structures. Note that we firstly grew pristine GaAs epi-layer free of native oxides to ensure the surface cleanness prior to the high-κ deposition, which is very important for (In)GaAs passivation.

We had carried out synchrotron radiation X-ray diffraction studies on MBE-HfO_2 on GaAs(001) and found that single crystal 5–6 nm thick MBE-HfO_2 was epitaxially grown on GaAs(001) in a monoclinic phase with excellent crystallinity [9]. However, the HfO_2 forms four domains, which surely cause leakage paths, inadequate for MOS application. Therefore, in this work, we deposited HfO_2 in a thickness of ~1.5–2 nm to just cover the whole GaAs surface but thin enough to prevent undesirable formation of multi-domains during anneals above 600 °C.

Fig. 1 shows the *C-Vs* of Ni/MBE-HfO_2/*p*-GaAs(001) MOSCAPs under different PDA conditions, measured at 500 Hz-1 MHz at room temperature. As shown in Fig. 1(a) and (b), when the annealing temperature raised from 850 °C to 900 °C, the frequency dispersion in accumulation region decreased from 14.8% to 12.4%. Moreover, the frequency dispersion was greatly reduced to 7.3% when the annealing time was extended from 10s to 30s, as shown in Fig. 1(c). These results suggest that our HfO_2/GaAs(001) interface possesses high thermal stability to 900 °C, the highest among all of the reported HfO_2/GaAs systems. Fig. 2(a) shows the characteristics of leakage current density with respect to electric field (*J-E*) for the MOSCAPs, the leakage current density remains as low as ~10^{-8}A/cm² at E < ± 3 (MV/cm), suggesting that the interface remains intact even after 900 °C annealing with duration time of 30s. From the cross-sectional scanning transmission electron microscopy (STEM) image on a 900 °C annealed MBE-HfO_2 on GaAs(001) shown in Fig. 2(b) it follows that the interface between the thin HfO_2 and GaAs remains atomically sharp. This also explains the low leakage current density in Fig. 2(a). The samples were subsequently undergone post metallization annealing (PMA) in forming gas (FG) at 400 °C for 5 min to improve the interfacial quality. This resulted in further reduction of the frequency dispersion down to 5.2%. Along with a sharp transition from accumulation to depletion, recognizable in *C-V* curves, this indicates that D_{it} is low under the mid-gap.

To investigate the D_{it} values around the mid-gap region, we measured the *C-Vs* at higher temperatures of 100 °C and 150 °C, as shown in Fig. 3(b) and (c). At 100 °C, the frequency dispersion became slightly larger, but the transitions of the *C-V* curves were still sharp, suggesting that the D_{it} is still maintained at a low value. But at 150 °C, the frequency-dependent flat-band shifts toward positive bias region were observed, indicating the existence of more traps distributed at the mid-gap, as more positive bias was needed to create the same amount of band-bending. However, unlike the inversion-like humps measured in the previously reported *C-Vs* of ALD- and molecular-beam-deposited (MBD)-Al_2O_3/GaAs at 150 °C [20,21], such mid-gap effects were not observed by measurements performed at elevated temperatures for MBE-HfO_2/*p*-GaAs(001) MOSCAPs.

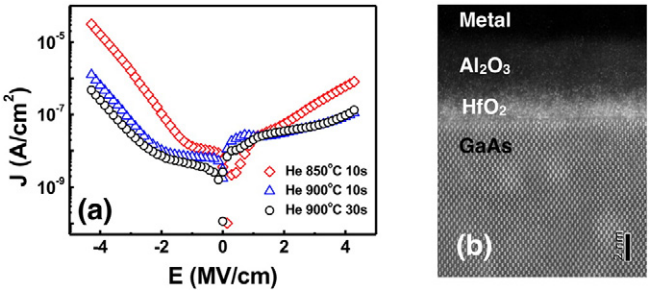

Fig. 2. (a) *J-E* characteristics of MBE-Al_2O_3/MBE-HfO_2/*p*-GaAs(001) MOSCAPs and (b)Cross-sectional HR-TEM image of MBE-Al_2O_3/MBE-HfO_2/GaAs(001).