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Research paper

Analysis of border and interfacial traps in ALD-Y_2O_3 and -Al_2O_3 on GaAs via electrical responses - A comparative study

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ABSTRACT

Y_2O_3 and Al_2O_3 were in-situ atomic layer deposited (ALD) on pristine GaAs(001)-4 × 6 reconstructed surfaces without surface pretreatments. We have studied the border and interfacial traps in both hetero-structures using the measured electrical responses. On the basis of frequency dispersion analysis of the capacitance-voltage (CV) characteristics, we conclude that Y_2O_3 has effectively passivated GaAs surface with a much lower interfacial trap density (D_{it}) than Al_2O_3 as the gate dielectric. The quasi-static CV and conductance measurements are in agreement with the above conclusion. We have demonstrated an excellent ALD-Y_2O_3/GaAs interface with low D_{it}'s of (0.5–2) × 10^{12} eV^{-1} cm^{-2} through the whole GaAs band gap without a mid-gap peak feature.

1. Introduction

GaAs and InGaAs are the leading candidates to replace Si as the n-channel material for future complementary metal-oxide-semiconductor field-effect-transistors (MOSFETs) because of their relatively high electron mobilities [1]. With a lattice constant of 5.87 Å, $In_{0.53}Ga_{0.47}As$ is more difficult to be integrated onto the Si(001) platform. In comparison, GaAs with a smaller lattice constant of 5.65 Å is easier to be grown on Si(001) (a lattice constant of 5.41 Å) [2]. Besides, with excellent uniformity and conformal coverage in nanometer thick film growth, atomic layer deposition (ALD) has been widely employed in depositing high-κ dielectrics for MOSFETs since the 45 nm node [3]. Therefore, as an urgent issue, intensive efforts in ALD high-κ dielectrics on GaAs(001) have been carried out to characterize and perfect these interfaces [4–10]. For the application of FET, more work needs be carried out to reduce border trap density and interfacial trap density under 2 × 10^{19} eV^{-1} cm^{-3} and 1 × 10^{12} eV^{-1} cm^{-2} respectively.

Frequency dispersion (FD) is an important index for characterizing oxide-semiconductor interfaces. As shown in Table 1, ALD-oxides on GaAs usually give a large FD in CV curves of the MOS capacitors (MOSCAPs), particularly on n-GaAs [6,11,12]. Research efforts have been carried out to explain the origin of the large FD in oxides/(In)GaAs interfaces. A model assuming an exponentially decaying spatial distribution of traps from the oxide/semiconductor interface into the bulk oxide layer explained the large FD of CVs at accumulation by the interfacial traps [13]. However, this model failed to explain the dispersion in the low frequency range and the temperature-dependent dispersion. Later, a distributed border trap model based on tunneling mechanism between the oxide/semiconductor interface and the trap states in gate dielectric accounted for the large FD of CVs and conductance (GV) at accumulation [14]. Chen et al. combined these two models to fit the CV and GV characteristics in depletion region to inversion region [15]. However, most reported high-κ/III-V systems yielded high trap densities up to 10^{13} eV^{-1} cm^{-2} as well as undesired interfacial native oxides, such that the corresponding analyses on capacitance-frequency (CF) characteristics led to unconvincing results [16,17]. The very few high-κ/GaAs(001) hetero-structures reported with low interfacial trap densities (D_{it}'s) are ultra-high vacuum (UHV) e-beam evaporated $Ga_2O_3(Gd_2O_3)$ and ALD-Y_2O_3 on GaAs(001) [18,19].

In this work, Y_2O_3 and Al_2O_3 were in-situ atomic-layer-deposited (ALD) on the molecular beam epitaxy (MBE) prepared GaAs(001)-4 × 6 reconstructed surfaces [11,20–22]. Note that the cleanliness of the GaAs surfaces without GaO_x, AsO_x, and other hydrocarbon contaminations, before the growth of ALD, were studied using in-situ X-ray photoelectron spectroscopy (XPS) [11]. The XPS also determined the band offsets between ALD-oxides and GaAs [22]. CVs, quasi-static CVs (QSCVs), GV, and CF characteristics were employed to analyze the border and interfacial traps at the ALD-Y_2O_3 and -Al_2O_3/GaAs(001) hetero-structures. Absence of mid-gap peak feature in the trap densities in

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Table 1
Comparison of frequency dispersion at accumulation between this work and other published works of ALD-oxides on GaAs(001).

Structure	F. D.		Reference
	p-type	n-type	
Al_2O_3/Y_2O_3/GaAs	4.4%	12.2%	This work
Al_2O_3/GaAs	9.0%	22.2%	This work
Al_2O_3/AlN/GaAs	13.4%	26.5%	[11]
Al_2O_3/GaAs	11.1%	52.8%	[6]

Y_2O_3/GaAs indicates an excellent quality of interface. The well-controlled oxides/GaAs interfaces using in-situ ALD approach [11,20–22] have provided an excellent platform for understanding the border and interfacial traps via their electrical responses under various measurements.

2. Experimental

The growth of ALD-Al_2O_3(5 nm)/ALD-Y_2O_3(2 nm) and ALD-Al_2O_3(5 nm) on freshly MBE grown p- and n-GaAs(001)-4 × 6 were carried out in a multi-chamber MBE/ALD/analyses UHV system [20]. An Al_2O_3 cap 5 nm-thick on top of the Y_2O_3/GaAs has prevented Y_2O_3 from moisture absorption in air. Optimized post deposition annealing (PDA) was conducted at 900 °C for 60s in N_2 for Y_2O_3/GaAs samples, and 550 °C 30s in N_2 followed by 850 °C 10s in He for Al_2O_3/GaAs samples, prior to the gate metal deposition. MOSCAPs were fabricated with e-beam evaporated Ni 100-nm thick 100 μm in diameter through a shadow mask as the gate electrode, and thermally evaporated Ti/Au as the backside electrode. We have measured the CVs from 500 kHz to 100 Hz at room temperature using an Agilent 4284A LCR meter, and QSCVs and current-voltage (I–V) characteristics in dark at room temperature using an Agilent 4156C. We have used the measured GV and QSCVs to calculate the interfacial trap densities (D_{it}'s).

Table 2
Maximum capacitance and estimated effective relative permittivity for oxides.

Structure	C_{max} at 5×10^5 Hz (μFcm^{-2})	C_{max} at 10^2 Hz (μFcm^{-2})	Effective relative permittivity
(5 nm)Al_2O_3/(2 nm)Y_2O_3/p-GaAs	1.277	1.34	12.2
(5 nm)Al_2O_3/p-GaAs	1.58	1.72	9.5

3. Results and discussion

Fig. 1(a) and (b) show the CVs of Y_2O_3 on p- and n-GaAs, while 1(c) and 1(d) show those of Al_2O_3 on p- and n-GaAs. FDs of 4% (12%) in accumulation were measured for Y_2O_3/p(n)-GaAs, smaller than those of 9% (22.2%) for Al_2O_3/p(n)-GaAs. The results are excellent, compared to other published works as listed in Table 1. The maximum capacitance and effective relative permittivity of the Al_2O_3/Y_2O_3 and Al_2O_3 stacks are listed in Table 2. We have studied the CF characteristics to understand the origin of frequency dispersion in accumulation, as shown in Fig. 2(a) and (b). With the tunneling mechanism to exchange charges between traps in the oxide layer and mobile carriers in the semiconductor, those traps closer to the interface can respond to higher input signal frequency in CV measurements. Therefore, it is critical to know the spatial distribution of the traps and its influence to the increment of frequency dispersion.

Traps that reside inside the dielectric possess a longer time constant than that of the interfacial traps. One can use the Wentzel-Kramers-

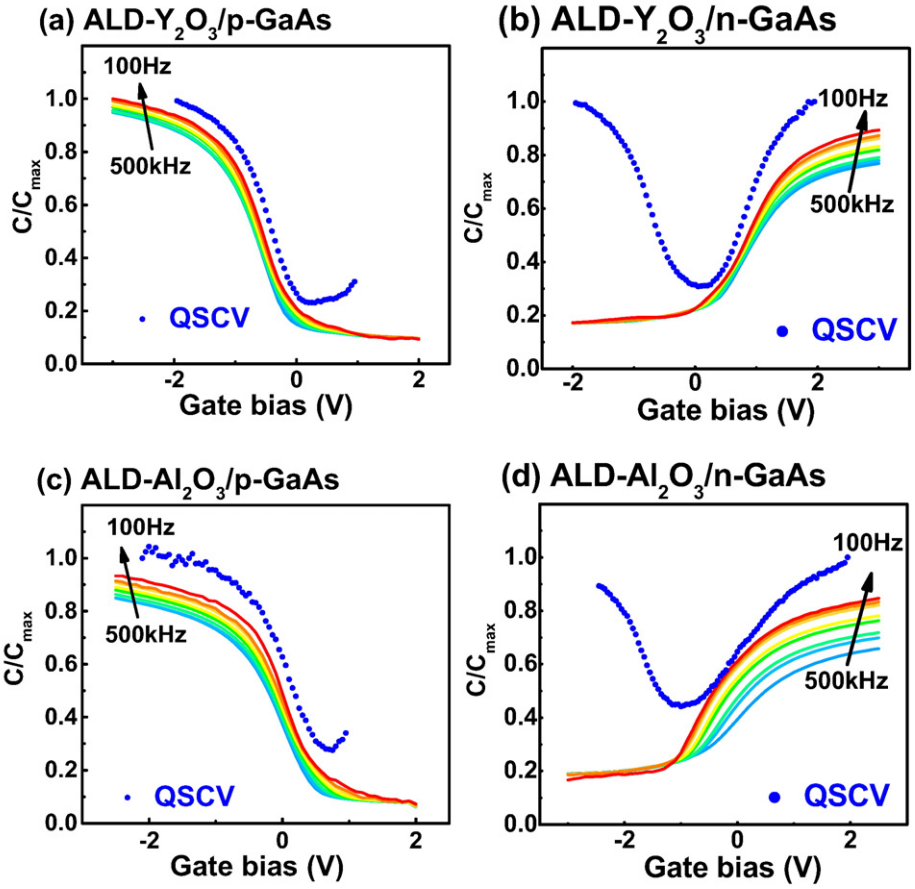

Fig. 1. CVs and QSCVs of MOSCAPs of ALD-Y_2O_3 on (a) p-type and (b) n-type GaAs, and ALD-Al_2O_3 on (c) p-type and (d) n-type GaAs.