Accepted Manuscript

Opportunity of dipole layer formation at non-SiO2 dielectric interfaces in two cases: Multi-cation systems and multi-anion systems



Jiayang Fei, Koji Kita

PII:	80167-9317(17)30232-0		
DOI:	doi: 10.1016/j.mee.2017.05.035		
Reference:	MEE 10588		
To appear in:	Microelectronic Engineering		
Received date:	19 February 2017		
Revised date:	12 May 2017		
Accepted date:	12 May 2017		

Please cite this article as: Jiayang Fei, Koji Kita, Opportunity of dipole layer formation at non-SiO2 dielectric interfaces in two cases: Multi-cation systems and multi-anion systems, *Microelectronic Engineering* (2017), doi: 10.1016/j.mee.2017.05.035

This is a PDF file of an unedited manuscript that has been accepted for publication. As a service to our customers we are providing this early version of the manuscript. The manuscript will undergo copyediting, typesetting, and review of the resulting proof before it is published in its final form. Please note that during the production process errors may be discovered which could affect the content, and all legal disclaimers that apply to the journal pertain.

ACCEPTED MANUSCRIPT

Opportunity of dipole layer formation at non-SiO₂ dielectric interfaces in two cases: multi-cation systems and multi-anion systems

Jiayang Fei and Koji Kita

Department of Materials Engineering, The University of Tokyo, 7-3-1 Hongo, Bunkyo-ku, Tokyo 113-8656, Japan E-mail address of corresponding author: jiavang@scio.t.u-tokyo.ac.jp

Abstract: This paper demonstrates possible dipole layer formation at non-SiO₂ interfaces in two cases: Al_2O_3/AlF_xO_y as an example of multi-anion systems and Al_2O_3/MgO as that of multi-cation systems. While unbalanced anion migration is considered as the origin at Al_2O_3/AlF_xO_y interface, caiton migration could play a dominant role in the charge separation at Al_2O_3/MgO interface annealed at higher temperature.

Keywords: dipole layer; gate dielectric interfaces; flatband voltage shift

1. Introduction

As threshold voltage tuning is important for advance metal-oxide-semiconductor field-effect transistors, dipole layer formed at gate dielectric interface has been recognized as a promising way to intentionally control the threshold voltage [1-4]. Extensive studies [5-10] have demonstrated dipole layer formation at high-k oxide/SiO₂ interfaces which could change the band alignment and shift the flatband voltage (V_{fb}) of MOS structures. However, reports on the dipole layer formation at the interfaces other than high-k/SiO₂ are quite limited. There are even reports suggesting dipole layer formation could be unique at high-k/SiO₂ interfaces [7] possibly because of the different structural characteristics between high-k oxides and SiO₂. In order to develop a strategy to design a MOS capacitors with desirable V_{fb} , understanding on the origin of dipole layer formation at general dielectric interfaces is necessary.

In this work, we studied dipole layer induced V_{fb} shift at non-SiO₂ interfaces, in the cases of Al_2O_3/AlF_xO_y and Al₂O₃/MgO, to demonstrate that even a non-SiO₂ dielectric interface can form an interface dipole layer. The oxide/fluoride interface was studied to clarify the effect of different kinds of anions since oxygen migration has been considered as the origin of dipole layer formation at high-k/SiO₂ interfaces [7]. In addition, the effect of F incorporation on V_{fb} needs to be understood because F has been used to improve the interface quality of gate stacks [11]. Al₂O₃/MgO interface was investigated to study the possible cation effect which is suggested as the origin of dipole layer formation at MgO/SiO2 interface [10]. Molecular dynamics (MD) simulation was also employed to reproduce the charge separation at Al₂O₃/AlF_xO_y and Al₂O₃/MgO. Further, the possible driving force of interface dipole layer formation at the simulated interfaces was discussed based on the interface atomic migration.

2. Experimental and Calculation Methods

The MOS capacitors with tri-layer dielectrics consisting of thermally-grown SiO_2 , dielectric 1 and dielectric 2 were fabricated. Dielectrics 1 and 2 as shown in TABLE I were

sequentially deposited by sputtering on p-type Si substrates covered with thermal oxides. Note that ~0.5 nm Al₂O₃ was capped on MgO to prevent moisture effect for Sample 3. Post deposition annealing (PDA) 1 and 2 were conducted in 0.1% O₂ ambient after the deposition of each layer. The final step was deposition of Au gate electrodes and Al back-side electrodes to form MOS capacitors. The flatband voltages were determined from the capacitance-voltage characteristics measured at a frequency of 1 MHz.

The molecular dynamics (MD) simulation was performed using a commercial simulation package Fujitsu SCIGRESS ME 2.1. Born-Mayer-Huggins potential, which includes point-to-point Columbic interaction between two atoms, van der Waals potential, and short-range repulsion, was employed,

$$V(r_{ij}) = \frac{q_i q_j}{4\pi\varepsilon_0 r_{ij}} - \frac{C_i C_j}{r_{ij}^6} + f\left(B_i + B_j\right) \left(\frac{A_i + A_j - r_{ij}}{B_i + B_j}\right),$$

where r_{ij} is the interatomic distance between the *i*-th and *j*-th atoms, f is a standard force of 1.154 kJ Å⁻¹ mol⁻¹, q is the amount of ionic charge, A is the ionic radii, B is the softness parameter, and C is the van der Waals coefficient. In this simulation, amorphous structures without defects have been studied. The completely ionic model (CIM) parameters of Al, O and F determined by Kawamura [12] were adopted in which the states of the ions are Al^{3+} , O^{2-} , and F. This simulation has been demonstrated to be effective in reproducing dipole layer formation at high-k/SiO₂ interfaces [13, 14]. The typical simulation process is as follows: first, amorphous Al₂O₃, AlF₃, and MgO blocks were obtained by melting the random structures with sizes of ~ $7 \times 7 \times 5$ nm³ at 4000K. The interfaces were obtained by stacking the amorphous blocks and annealed by the isothermal-isobaric MD calculation for 10 ps, thermostated at 1000 K by speed scaling with keeping the pressure at 1 atm; finally, the structure was cooled from 1000 to 300 K within 30 ps and maintained at 300 K for another 10 ps.

TABLE I. List of dielectrics and PDA temperatures. ~ 0.5 nm Al₂O₃ was capped on MgO to prevent moisture effect for Sample 3.

	<u> </u>			
	Layer 1	PDA 1	Layer 2	PDA 2
	(bottom)	$T(^{o}C)$	(top)	$T(^{o}C)$
Sample 1 Reference 1	Al ₂ FO _{2.5}	400	Al ₂ O ₃	500
Sample 2 Reference 2	Al ₂ O ₃	600	AlFO -	400
Sample 3 Reference 3	Al ₂ O ₃	w/o, 600, 700, or 800	MgO(cap) -	600 or 800

3. Results and Discussions

Download English Version:

https://daneshyari.com/en/article/4970851

Download Persian Version:

https://daneshyari.com/article/4970851

Daneshyari.com