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Interaction of Work Function tuning and Negative Bias Temperature Instability for future nodes

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I.Introduction

Future nodes will increasingly rely on the effective workfunction (EWF) tuning to achieve the desired transistor V_T as FinFET doping is poorly effective. Workfunction tuning is a key parameter for HK/MG devices in Replacement Metal Gate (RMG) architecture [1,2]. The metal gate thickness and chemistry control the effective workfunction (EWF, or transistor V_{fb}/V_T assuming negligible dielectric charge) of the RMG stack. The intrinsic reliability is controlled by gate dielectric thickness, threshold voltage EWF/V_T, as well as RMG key manufacturing steps[3-6]. Historically, it has always been challenging to isolate the effects of workfunction (i.e., barrier height [7]) from dielectric/dipole charge (point defects). In a nutshell, the high thermal budget during processing and / or the small transistor dimensions may confound the information on dielectric charges [8], actual gate stack changes (interfacial SiO_2 regrowth, scavenging) and band alignment. Additionally, techniques like internal photo emission are not suitable for small finfet structures [9] and therefore V_T has been the tool of choice for band alignment extraction.
This work demonstrates an original technique to extract band alignment on PFET using valence band electron tunneling (VBET) in next generation FinFET technology nodes. This work is divided as follows. First the EWF extraction technique and its link to actual V_T are investigated using a unique combination of CV/IV techniques. The ~400meV band alignment change takes place without an appreciable change in interfacial layer quality, thickness nor stress-induced-like defects. Such a large EWF modulation however impacts the NBTI significantly. The band alignment and NBTI correlation is further investigated in gate stacks where both the interfacial layer and the EWF are changed because of thermal annealing. Finally the role of bulk defects and band alignment is discussed using charge recovery experiments.

II. Devices and experiments

14nm node FinFET and planar devices were considered in this experiment where the metal gate (MG) workfunction, chemistry and thermal budgets have been greatly varied. In one additional experiment the EWF has been modulated using capping layers [10]. Large area capacitors have been used to collect CV and IV traces in accumulation and inversion to extract V_{fb}, the equivalent inversion capacitance (T_{inv}) and the equivalent gate leakage thickness (TOXGL) [11]. The negative bias temperature instability (NBTI) has been measured in nominal devices technology using standard Stress-Measure-Stress technique using drain current in linear regime for sensing and constant voltage stress for stress. Additional experiments using an inline Voltage Ramp Stress [19] were done.

III. Band alignment extraction method using conventional CV/IV

A controlled experiment using unipolar CMOS was designed to investigate the defect and EWF interaction. “Unipolar” CMOS refers to NFET/PFET transistors featuring the same metal gate chemistry on the same wafer. As an example, in a low EWF unipolar CMOS, the NFET V_T is on target while the PFET is very high. As it will be clear, from a defect characterization point of view, this approach has the inherent advantages of both NFET and PFET. Gate leakage can be effectively used to scan HK defects in a wide dielectric bandgap (positive and negative V_G’s) with the same MG process, thus allowing the extraction of any non-ideal behavior.
Fig.1a shows the CV results where the EWF modulates the flatband voltage V_{fb} by >400meV for NFET - a low EWF results in a low V_{fb} while a higher EWF would result in a higher V_{fb}. The same observation holds true for PFET. Once the change in silicon doping potential is taken into account[1] the EWF extracted from unipolar NFET and PFET devices on the same wafer show a 1:1 correlation (Fig.1b), implying that extraction method is robust and consistent.
The carrier separation experiments of Fig.2a and Fig 2b provide additional information on band alignment and the nature of defects. During a carrier separation all the MOSFET currents at gate / substrate / SD are recorded and compared. In these thin films leakage occurs because of the coupling between available states and empty states, either due to defects (interface states [13], SILC-like bulk defects [14]) or a change in band structure. In the following we will use the valence band tunneling to quantify the band alignment between Si and the metal gate as the near-ideality I_{sub} and I_g currents in inversion provide additional evidence that no additional SILC-like defects nor interface states are present for both NFET and PFET. Separate mobility and charge pumping experiments (not shown) demonstrate that the MG process does not provide additional scattering defects at the Si interface (i.e., no IL SiO_2 perturbation by changing the EWF metal).
The bandgap modulation for NFET is highlighted in Fig.2a. The substrate current I_{sub} is proportional to valence band Ev(Si) alignment to MG while the gate current I_G is mostly sensitive to the inversion layer charge (i.e., V_T/EWF) [15][16]. Changing EWF by ~400mV provides a significant change in gate current I_G while the substrate current I_{sub} is unchanged suggesting that the MG

[1] After carefully subtracting any parasitic capacitance contributions, the silicon potential can be extracted using the NCSU CVC software [12] from Hauser et al.

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