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Research paper

High-K metal gate stacks with ultra-thin interfacial layers formed by low temperature microwave-based plasma oxidation

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ABSTRACT

Ultra-thin interfacial silicon oxide layers are grown by microwave-based plasma oxidation at temperatures below 200 °C. The influence of plasma gas composition and plasma pulsing on layer properties is tested. The oxides are compared to standard thermally grown oxide and wet chemical oxide. Layer properties are evaluated by x-ray photo electron spectroscopy and are electrically characterized by means of TiN/HfO_2/SiO_2 high-k metal gate stacks.

1. Introduction

In high-k metal gate (HKMG) transistor technology, the formation of ultra-thin SiO_2 or SiON-based interface layers between gate dielectric and channel material is one of the key processes to control transistor performance. Thermal oxidation generates a high quality SiO_2/Si interface, but also induces a high thermal budget to the underlying substrate with temperatures of 850 °C or more. This temperature is critical, especially in monolithic 3D integration that requires a thermal budget limitation of 500 °C for processing of a second active layer over an existing transistor level [1]. Microwave-based low temperature plasma oxidation is a suitable technology to oxidize Ge [2] as well as Si in the requested temperature regime. Here we demonstrate that this technique enables the formation of high-quality interface layers in HKMG stacks at process temperatures well below 200 °C. The influence of plasma composition and plasma pulsing is tested and compared to standard thermally grown oxide and wet chemical oxide. The plasma nitridation capability to further improve the oxides is explicitly not reviewed in this contribution to demonstrate only the advantages of the low-temperature oxide growth [2].

2. Experimental

Firstly, 300 mm p-type silicon wafers were pre-cleaned using a SC1/DHF/HCl sequence which results in a well-defined 0.4 nm wet chemical oxide. This is directly followed by low temperature microwave-based anodic plasma oxidation to form interfacial layers between 0.8 nm and 2.0 nm. More details on the plasma oxidation and the apparatus itself can be found elsewhere [3]. The plasma was run either in continuous or pulsed mode using gas mixtures of H_2/He/O_2, H_2/O_2, or pure O_2. Reference samples were thermal oxides grown at 850 °C in diluted O_2 by rapid thermal oxidation (RTO) and the wet chemical oxide after pre-clean (ChemOx). For all interfacial layers, thickness, composition, and binding configuration were extracted from x-ray photo electron spectroscopy (XPS). For the fabrication of high-k metal gate structures, 4.8 nm hafnium dioxide (HfO_2) was deposited by atomic layer deposition using chlorine-based precursor chemistry followed by chemical vapor deposition of titanium nitride (TiN) metal gates. The stack is covered by amorphous silicon that acts as hard mask. No additional post-treatments such as post deposition annealing were applied. The gates were patterned by lithography and a sequence of dry etching of the hard mask and wet etching of the TiN gate electrodes. This two-step etching approach allows the gentle patterning of the TiN gates without altering the substrate adjacent to the gate stacks by the dry etching plasma.

3. Results and discussion

Directly after interface formation by plasma oxidation or RTO, wafers were analyzed by XPS to investigate binding configuration and extract the layer thickness from intensity ratios of substrate and SiO_2 layer photoelectron peaks. The methodology for thickness determination of thin oxides and nitride oxides by XPS is described in reference [4]. The XPS spectra of all studied low temperature plasma oxides show two main features (Fig. 1).

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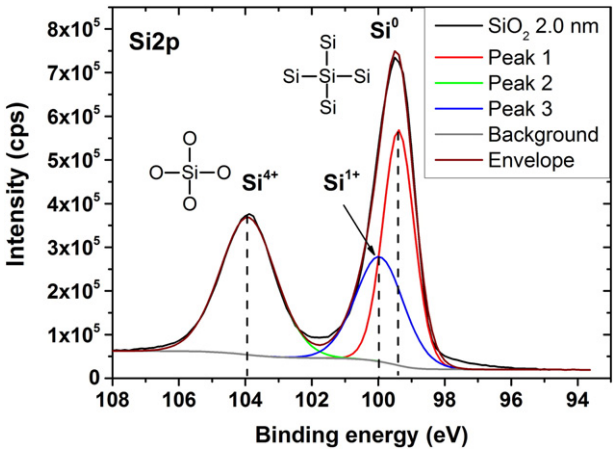

Fig. 1. Si 2p XPS spectrum layers grown by plasma oxidation in $H_2/He/O_2$. The peak positions indicate stoichiometric SiO_2 on silicon substrate.

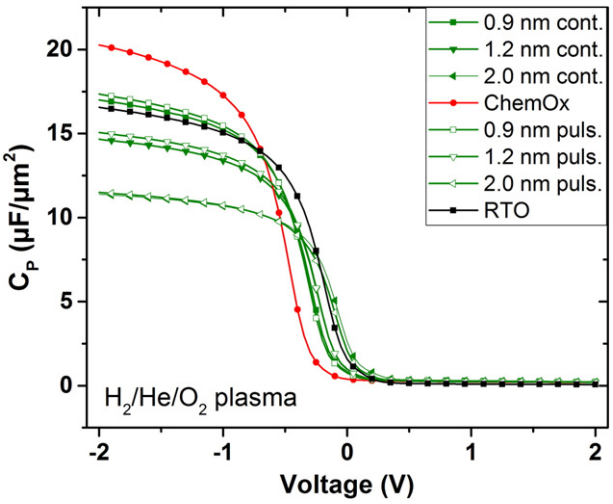

Fig. 3. High frequency CV curves at 10 kHz of HKMG stacks with interfaces of 0.9, 1.2 and 2.0 nm grown in $H_2/He/O_2$ using continuous or pulsed plasma modes.

The peak at 99.4 eV corresponds to the Si^0 state of the Si substrate where the Si atoms are surrounded by four Si neighbors. In all XPS spectra, this substrate peak is used as internal reference to compensate for charging effects. The Si^{4+} peak at 103.9 eV originates from fully oxidized Si with four oxygen neighbors. Spectra deconvolution reveals a third peak at 100.0 eV due to the substrate $Si2p^{3/2}$ and $Si2p^{1/2}$ orbital splitting [5]. This peak can contain also a small fraction of Si^{1+} sub-oxides at the SiO_2/Si interface that cannot be resolved here.

This conclusion is derived from the fact that the peak slightly shifts for the different oxides what would not be the case if the peak originates only from substrate orbital splitting. Photoelectron energies of the Si^{4+} peaks are highest for both oxides that are grown in hydrogen containing plasma (H_2/O_2 and $H_2/He/O_2$) whereas the Si^{4+} peak is slightly shifted to lower energies by 0.1 eV for O_2 plasma and RTO and by 0.2 eV for ChemOx (Fig. 2). This change in the Si^{4+} binding energy is mainly an effect of layer thickness when with increasing thickness the peak shifts to higher energies of the SiO_2 bulk layer. The Si^{1+} photoelectron energy of RTO is 0.3 eV higher compared to the plasma oxides and ChemOx which might originate from a higher ratio of sub-oxides in the layer.

Capacitance-voltage (CV) characteristics were measured on high-k metal gate stacks with interface layers between 0.9 nm and 2.0 nm and a constant thickness of 4.8 nm HfO_2 topped by a TiN gate electrode. The capacitance equivalent thickness (CET) is calculated from the maximum capacitance in accumulation. The CET values agree very well (<5%) with the theoretical CET of the stacks taking into account the interfacial SiO_2 thickness measured by XPS and the constant CET of the HfO_2 layer (1.05 nm). High frequency CV curves of stacks with interface layers grown in pulsed or continuous mode $H_2/He/O_2$ plasma are shown in Fig. 3. Similar to the RTO and ChemOx reference interfaces no trap-related distortion of the CV curves can be observed. Hysteresis of the CV curves (not shown here) are in the range of 10–20 mV for 0.9 to 1.2 nm interfaces with some advantages for the plasma oxidation. For stacks with 2.0 nm interface thickness no hysteresis can be measured. Since hysteresis is typically considered as reversible charging of defects in the oxide close to the interface, this effect here is mainly caused by defects in the HfO_2 close to the SiO_2 interface layer. With thicker SiO_2 the hysteresis effect is reduced since charges are further away from the channel and can be less effectively accessed by tunneling through the SiO_2 interface layer.

Fig. 4 summarizes the flatband voltages (V_{FB}) extracted experimentally from high frequency CV curves at 10 kHz using the methodology described in [6]. Comparing V_{FB} at a constant CET of 2.1 nm, H_2/O_2 plasma oxide shows a V_{FB} of around +0.10 V whereas all other plasma oxides have V_{FB} values around 0 V. Both are significantly lower as the +0.20 V of the 1.1 nm RTO reference. The ChemOx has no

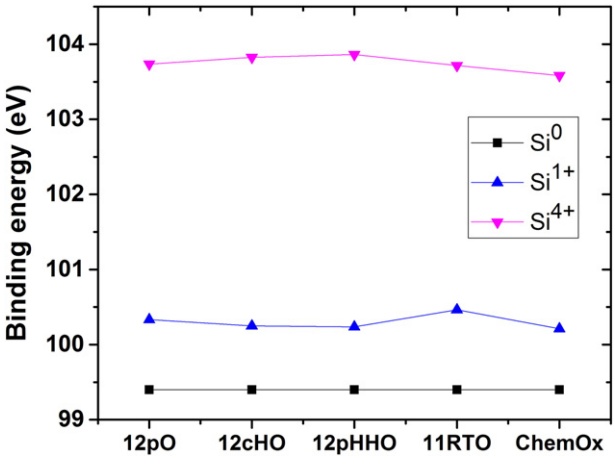

Fig. 2. Comparison of Si 2p XPS peak positions of oxides with 1.2 nm thickness grown in pulsed O_2 (12pO), in continuous H_2/O_2 (12cHO) and pulsed $H_2/He/O_2$ (12pHHO) plasma, the reference 1.1 nm RTO (11RTO) and wet chemical oxide (ChemOx).

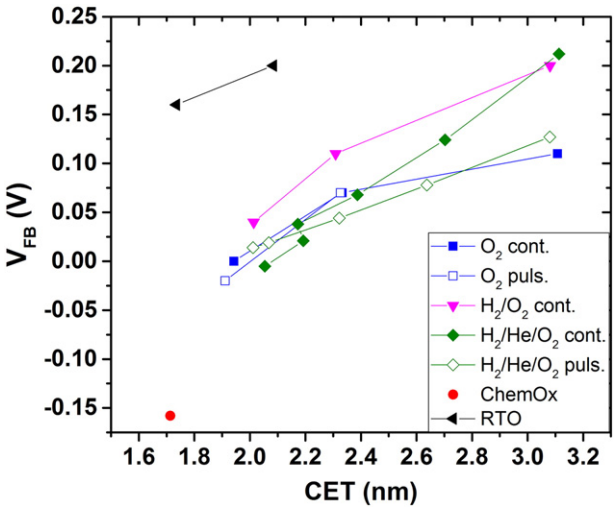

Fig. 4. Flatband voltage (V_{FB}) extracted from CV curves. Plasma oxides are shifted to more negative values compared to thermal RTO, but less than wet chemical oxide.