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Research paper

Improved performance of gate-last FDSOI tunnel field-effect-transistors (TFETs) with modulating Al_2O_3 composition in atomic layer deposited $HfAlO_x$ gate dielectrics

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ABSTRACT

We have studied the electrical characteristics of both n-type and p-type fully depleted silicon on insulator (FD-SOI) tunnel field-effect transistors (TFETs) by modulating Al_2O_3 fraction (25%, 50%) within atomic layer deposited $HfAlO_x$ gate dielectric. Compared to HfO_2 alone, lower subthreshold swing (S.S), higher I_{on}/I_{off}, and stronger threshold voltage (V_{th}) immunity against electrical stress are obtained for both n-type and p-type TFETs by adopting nano-laminated atomic layer deposited $HfAlO_x$, attributed to the increased band gap and interfacial layer scavenging effect.

1. Introduction

The metal oxide semiconductor field effect transistor (MOSFET) has been scaled down for the performance enhancement. Simultaneously, it also needs to lower the power consumption consisting of the standby power and the operation power [1–3]. The transistor power consumption can be reduced by lowering the off-leakage current (I_{off}), the supply voltage (V_{dd}), and subthreshold swing (S.S). Since the conventional MOSFET has the limit to lower the S.S (<60 mV/dec at T = 300 K) due to the thermal diffusion current, alternative tunnel field effect transistor (TFET) has been considerably investigated as a promising candidate device for low power applications [4–6]. It can provide steeper subthreshold swing, low off current, scalability and process compatibility to complementary metal oxide semiconductor (CMOS) integration. However, it suffers from low drive current due to the band-to-band tunneling mechanism. Therefore, small band-gap materials such as SiGe and Ge are proposed to enhance the tunneling current [7–8]. For improving subthreshold swing and on current characteristics together, gate leakage current should be carefully considered. The gate insulator with high gate leakage current adversely affects the channel current when drain voltage becomes low. The material modulation could improve leakage behavior further in the TFETs. Particularly, $HfAlO_x$ is expected to suppress the leakage current further because Al_2O_3 is relative wide band gap material while HfO_2 is with high dielectric constant [9–10].

In this study, we demonstrate both n-type and p-type Si TFETs with Al_2O_3-modulated ALD $HfAlO_x$ gate dielectric. The effects of Al_2O_3 composition modulation on the performance and reliability of the TFETs are systemically characterized.

2. Experiment

Tunnel field effect transistor (TFET) with W/L = 5 μm × 5 μm was fabricated on the 6-inch p-type silicon on insulator (SOI) substrate. The thickness of silicon dioxide as a buried oxide layer is 375 nm while silicon as a substrate is 100 nm. The SOI was thinned to 50 nm via sequential processes of oxidation and wet etching with 7:1 buffered hydrofluoric acid (BHF). The following was the active area formation (width/length = 5 μm/5 μm). BF_2 and As was implanted at 10 KeV with dose of 3.0×10^{14} cm^{-2} into the source and drain regions, respectively. After dopant activation annealing at 950 °C for 5 s, HfO_2, $HfAlO_x$ (Al 25%, HAO) and $HfAlO_x$ (Al 50%, HAO) as gate dielectrics were deposited at 250 °C with 5 nm thickness on the Si substrate by atomic layer deposition (ALD). Tetrakis (ethyl-methylamido) hafnium (TEMAHf) and Tri-methyl-aluminum (TMA) precursors were used for HfO_2 and Al_2O_3 precursors while H_2O was used as an oxidant for films. The Al_2O_3 composition within $HfAlO_x$ gate dielectric was modulated by changing HfO_2 and Al_2O_3 cycles, and detail features are shown in the Table 1. The 150 nm-thick TiN as a gate electrode

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Table 1
The process information of ALD gate dielectrics: HfO_2 and $HfAlO_x$ deposition cycles, deposition rate, and physical thickness. Al composition is defined by the number of cycle steps.

Dielectrics	Number of HfO_2 cycles	Number of Al_2O_3 cycles	Deposition rate (Å/cycle)	Physical thickness (nm)
HfO_2	4	0	1.02	4.9
HAO (Al 25%)	3	1	1.07	5.1
HAO (Al 50%)	2	2	1.12	5.0

was DC-sputtered, and Ti/Al/TiN multi-layers as contact metal were deposited with 50/350/50 nm thickness. After the subsequent lithographic processes, the final forming gas annealing was carried out at 400 °C for 30 min at H_2/N_2 mixture ambient. The transistor characteristics was measured by Keithley 4200 SCS and capacitance measured by Agilent 4294A. The interface state density (D_{it}) was extracted by the charge pumping measurement. The transmission electron microscope (TEM, JEM-2100F) was used for interfacial layer (IL) and high-*k* layer thickness.

3. Result and discussion

Fig. 1 shows the I_d-V_g (a) and I_d-V_d (b) characteristics of n-type TFETs with three dielectrics, respectively. TFET with HAO (Al 25%) shows higher drain current than that of HfO_2 TFET while HAO (Al 50%) TFET shows the lowest current level due to higher Al_2O_3 fraction. In addition, $HfAlO_x$ gate dielectric improves the on/off current ratio. The HfO_2-TFET, HAO (Al 25%)-TFET, and HAO (Al 50%)-TFETs show 1.7×10^5, 3.1×10^5, and 1.9×10^5 current ratio, respectively. The HAO gate dielectric with Al 25% seems to be optimal. The threshold voltage (V_{th}) of each devices are measured to be 1.21 V, 1.14 V and 1.62 V for HfO_2, HAO (Al 25%), and HAO (Al 50%)-TFETs, respectively. Fig. 2 compares the point subthreshold swing of the TFETs having HfO_2, HAO (Al 25%) and HAO (Al 50%) with respect to gate voltage. Compared to HfO_2 TFET (215 mV/dec), improved subthreshold swing (S.S) is attained with HAO (Al 25%) TFET (156 mV/dec) and HAO (Al 50%) TFET (199 mV/dec). Fig. 3 shows the I_d-V_g (a) and I_d-V_d (b) characteristics of p-type TFETs with three dielectrics, respectively. Similar to n-type TFET, HAO (Al 25%) p-type TFET shows higher on-current and lower off current. Unlike n-type TFET transfer behavior, in p-type TFET, degradation in current of HAO (Al 50%) becomes smaller. The on/off current ratio of HfO_2, HAO (Al 25%), and HAO (Al 50%) TFET

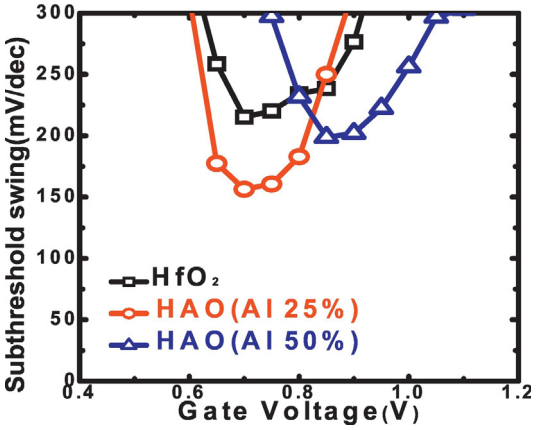

Fig. 2. Point subthreshold swing of n-type TFETs as a function of gate voltage.

are 6.6×10^5, 9.4×10^5, and 8.7×10^5, respectively. Better output characteristic is observed with HAO (Al 25%). The threshold voltage of each devices are measured to be −0.95 V, −0.96 V and −1.11 V for HfO_2, HAO (Al 25%), and HAO (Al 50%)-TFETs, respectively. Fig. 4 compares the point subthreshold swing of the p-type TFETs having HfO_2 and HAO gate insulators. Compared to HfO_2 TFET, point S.S of HAO TFET is also improved. The lowest S.S with 75 mV/dec is attained from HAO (Al 25%) TFET. The S.S of HAO (Al 50%) and HfO_2 TFET are with 128 mV/dec and 141 mV/dec, respectively. Fig. 5 represents capacitance-voltage behaviors (a) and equivalent oxide thickness (EOT)/inversion thickness (T_{inv}) (b) of TFETs, respectively. Increasing Al_2O_3 fraction within $HfAlO_x$ lowers the oxide capacitance. Maximum oxide capacitance of each devices is attained with 2.14 μF/cm^2, 2.03 μF/cm^2 and 1.94 μF/cm^2 for HfO_2, HAO (Al 25%), and HAO (Al 50%) cases, respectively. Nevertheless, HAO (Al 25%) TFET shows higher current than that of HfO_2 TFET, indicating another term affecting drain current such as impact from interfacial layer (IL) trap. The equivalent oxide thickness (EOT) is attained with 1.61 nm, 1.69 nm and 1.78 nm for HfO_2, HAO (Al 25%), and HAO (Al 50%) cases, respectively, while inversion thickness (T_{inv}) is with 1.69 nm, 1.77 nm and 1.89 nm for HfO_2, HAO (Al 25%), and HAO (Al 50%) TFETs. In order to investigate the effect of interfacial layer trap, charge pumping characterization was carried out. Fig. 6 compares the charge pumping current (I_{cp}) (a) and interface trap charge density (N_{it}) (b) of TFETs with HfO_2, HAO (Al 25%), and HAO (Al 50%). The maximum I_{cp} of each devices are measured with 200 nA, 120 nA and 144 nA for HfO_2, HAO (Al 25%), and HAO (Al 50%) cases,

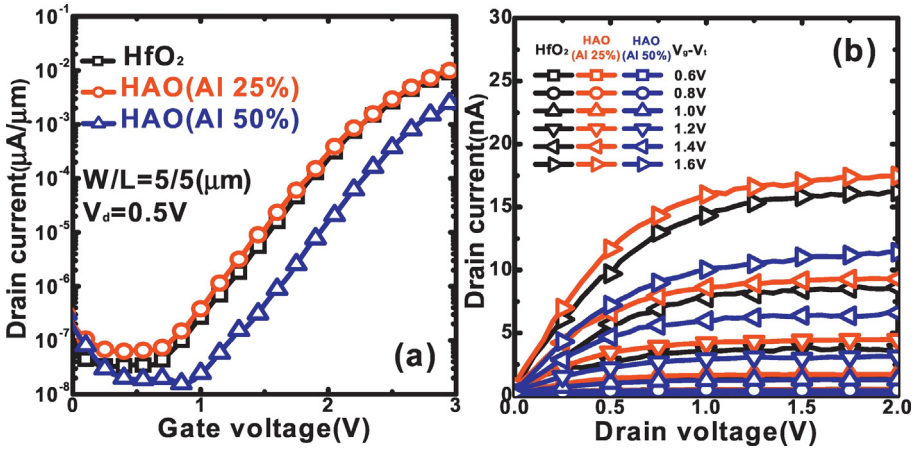

Fig. 1. I_d-V_g (a) and I_d-V_d (b) characteristics of n-type SOI TFETs with HfO_2, $HfAlO_x$ (Al 25%) and $HfAlO_x$ (Al 50%), respectively.