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Research paper

Enhancement of effective dielectric constant using high-temperature mixed and sub-nano-laminated atomic layer deposited Y_2O_3/Al_2O_3 on GaAs(001)

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ABSTRACT

In-situ atomic layer deposition (ALD) Y_2O_3/Al_2O_3 in bi-layered and sub-nano-laminated structures were stacked on pristine GaAs(001) substrates for fabricating metal-oxide-semiconductor capacitors. The bi-layered Y_2O_3/Al_2O_3 showed an enhanced effective dielectric constant from 11.1 to 15.6 in capacitance-voltage characteristics with post deposition annealing to 900 °C. No new oxide phase formed as carefully examined using synchrotron radiation X-ray diffraction and cross-sectional high-resolution scanning tunneling electron microscopy. We designed and grew sub-nano-laminated Y_2O_3/Al_2O_3 multi-layers to simulate the mixing of gate oxides, and observed an enhanced dielectric constant of 14.8 for the as-deposited sample. Both high-temperature mixed and sub-nano-laminated ALD Y_2O_3/Al_2O_3 exhibit high dielectric constant, low leakage current ~10^{-8} A/cm^2 and low interfacial trap density with GaAs(001), promising for high κ applications in future GaAs metal-oxide-semiconductor devices.

1. Introduction

Si-based metal-oxide-semiconductor field-effect-transistors (MOSFETs) have undergone extreme scaling in the past few decades fulfilling Moore's law. As the production for the 7 nm node and research for the ultimate complementary MOS (CMOS) is around the corner, diverse solutions have been enabled for future integrated circuits [1–3]. Among them, integrating high carrier mobility III-V compound semiconductors onto the Si(001) platform is a very promising approach, as it provides an effective way to enhance the device performance having less power consumption without the need for further aggressive scaling [4]. Among the III-Vs, GaAs has a closer bandgap and lattice constant to those of Si. Nevertheless, three major issues for realizing high performance GaAs inversion-channel devices are an oxide with an enhanced high dielectric constant (κ) on GaAs, a low interfacial trap density (D_{it}) at oxide/GaAs(001) interface, and thermal stability at temperatures higher than 850–900 °C.

Previously, we have demonstrated the growth of single crystalline Y_2O_3(110) thin films onto GaAs(001) wafers using *in-situ* atomic layer deposition (ALD), [5,6] with a dielectric constant of Y_2O_3 being ~16. The high dielectric constant of Y_2O_3 is beneficial for equivalent oxide thickness (EOT) scaling, while retaining reasonable physical thickness to prevent large gate tunneling current. The Y_2O_3/GaAs hetero-structure has a type-I band alignment (straddling gap) with large conduction and valence band offsets reported as 2.21 eV and 2.14 eV, respectively [7]. Furthermore and very importantly, in our previous work, the Y_2O_3/GaAs interface shows excellent electrical properties including a low D_{it} of (1–2) × 10^{12} eV^{-1} cm^{-2}, as extracted by quasi-static capacitance-voltage (QSCV) curves and a small frequency dispersion of 7% in the capacitance-voltage (CV) curves from 1 MHz to 100 Hz, as measured on p-type GaAs MOS capacitors (MOSCAPs) [5,6]. The gate leakage current density is below 10^{-8} A/cm^2 because of the excellent crystallinity of Y_2O_3, as well as the appropriate conduction band and valence band offsets for the Y_2O_3/GaAs hetero-structure. The attainment of high temperature thermal stability at 900 °C is a must for the gate-first device processing. We would like to emphasize again that those excellent results mentioned above are for GaAs in (001) orientation, rather than (110), (111) or others. Since Y_2O_3 absorbs moisture easily, which causes oxide degradation and affects its electrical performance, a single Y_2O_3

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layer acting as the gate oxide is not preferred. During our sample preparation, usually an ALD Al_2O_3 capping layer was employed to prevent the moisture absorption of Y_2O_3 when the sample was exposed to air for processing. However, the moderate κ value of Al_2O_3 ~8.5 is disadvantageous of pushing EOT scaling.

Recently, Y. Liu et al. and X. Wang et al. have published effective passivation of GaAs with D_{it} below 10^{12} eV^{-1} cm^{-2} using ALD rare-earth oxides. However, their work was demonstrated in (111)A orientation and the total gate oxide thicknesses were rather thick exceeding 10 nm, which was also disadvantageous for EOT scaling [8,9]. T. Aoki et al. reported Al_2O_3/AlN passivated GaAs(001) with D_{it} ~ (1–4) × 10^{12} eV^{-1} cm^{-2}, but the oxide stack exhibited only a moderate κ value [10]. Y. C. Chang et al. also reported Al_2O_3 passivated Ga-rich GaAs(001) achieving D_{it} ~1 × 10^{12} eV^{-1} cm^{-2}, but the CET was about 4 nm [11]. Y. H. Chang et al. and Y. H. Lin et al. have demonstrated effective passivation of $In_{0.2}Ga_{0.8}As$(001) and GaAs(001) using ALD high-κ HfAlO/HfO_2 and Al_2O_3/Y_2O_3 respectively with low D_{it} and CET below 3 nm [12,13].

In this work, we have discovered a great enhancement of effective dielectric constant for the gate stacks of ALD-Al_2O_3 (5.0 nm)/ALD-Y_2O_3 (2.3 nm) on p-type GaAs(001) samples with annealing temperature exceeding 900 °C, which was revealed by the accumulation capacitance measured in the CV curves. Initially, we speculated that a higher κ value came from the formation of a new oxide compound. Nevertheless, the efforts using synchrotron radiation X-ray diffraction (XRD) and high-resolution scanning transmission electron microscopy (STEM) have not found evidences of crystalline phases. The bi-layered oxides of single crystalline Y_2O_3(110) and amorphous Al_2O_3 became amorphous with mixed Y_2O_3/Al_2O_3 after 900 °C post deposition annealing (PDA). Inspired by this result, we further designed sub-nano-laminates (snl) of Y_2O_3/Al_2O_3 by the approach of ALD super-cycle intentionally to form an amorphous mixed Y_2O_3/Al_2O_3 layer on p-GaAs(001) for MOSCAPs, in which an enhanced κ value was also observed. Moreover, the CV curves (1 MHz to 100 Hz) for the as-deposited sample have shown excellent characteristics with low gate leakage current densities.

2. Experimental

In our multi-chamber UHV system [14], p-GaAs epi-layers doped with Be were grown on Zn-doped p-GaAs(001) wafers two-inch in diameter in a solid-source GaAs-based MBE chamber. The samples were *in-situ* transferred under ~10^{-10} Torr to an As-free oxide-MBE chamber, and annealed to ~560 °C for attaining 4 × 6 reconstructed surfaces as confirmed by reflection high-energy electron diffraction (RHEED) patterns.

Then, the samples were *in-situ* transferred to the thermal ALD reactor for oxide deposition. Two different gate oxide stacks were prepared; structure A (a bi-layered structure) had 16 cycles of Y_2O_3 followed by 56 cycles of Al_2O_3, and structure B had 24 super-cycles (sub-nano-laminated multi-layers), with each super-cycle consisting of 3 cycles of Y_2O_3 followed by 3 cycles of Al_2O_3. The growth of Y_2O_3 was *via* the surface reactions of tris(ethylcyclopentadienyl)yttrium(III) (Y(EtCp)$_3$) and H_2O precursors with the substrate temperature of 270 °C. The growth of Al_2O_3 was *via* the surface reactions of trimethylaluminum (TMA) and H_2O precursors with the substrate temperature of 320 °C. The growth rates of Y_2O_3 and Al_2O_3 were measured as 1.69 Å/cycle and 0.9 Å/cycle respectively. Fig. 1 shows the schematic sample structures.

Post deposition rapid thermal annealings (RTA) were *ex-situ* performed on the samples, followed by evaporating Ni dots through a shadow mask with 100 μm in diameter as the top gate, and Ti/Au as the back contact electrode for the electrical measurements. We have measured the CV characteristics using Agilent 4284A Precision LCR meter, and the gate leakage current using Agilent 4156C Precision Semiconductor Parameter Analyzer. We have used the X-ray diffraction (XRD) and X-ray reflectivity (XRR) to measure the crystallography and the thickness of the samples at National Synchrotron Radiation Research Center. We have applied a focused ion beam (FIB) technique to prepare the STEM samples. A spherical aberration (Cs) corrected STEM (JEOL JEM-ARM200F) was utilized to study the cross-sectional images of the samples at an accelerating voltage of 200 kV.

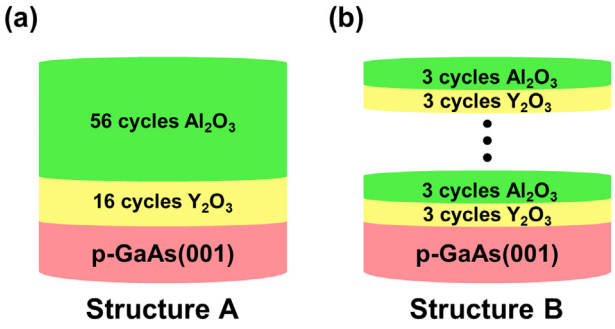

Fig. 1. Schematic diagrams for (a) bi-layered (structure A) and (b) 24 super-cycles sub-nano-laminated (structure B) ALD Y_2O_3/Al_2O_3 on GaAs(001).

3. Results and discussion

Fig. 2(a)–(c) show the CV curves for samples of structure A of as-deposited, post-deposition annealed at 850 °C and at 900 °C. The frequency dispersion in the accumulation region for these three samples are 28.4%, 10.3%, and 7.4%, respectively for the probed frequency between 1 MHz and 100 Hz. As shown, the 900 °C annealing optimizes the Y_2O_3/GaAs interface, as demonstrated by the smallest frequency dispersion in the accumulation and depletion regions [5]. The frequency dispersion for the as-deposited sample in higher frequency range (>100 kHz) probably caused by imperfection of back Ohmic contact [15]. We have checked the inversion behavior of the MOSCAP under positive bias by the minimum capacitance C_{min} [16,17]. An ideal CV curve simulated using MATLAB for the 900 °C-annealed sample by its structural and material parameters including GaAs doping concentration ~7 × 10^{17} cm^{-3} suggests a C_{min} ~0.19 μF/cm^2 which fits the experimental data. Moreover, an abrupt increase of the accumulation capacitance appeared between the samples annealed at 850 °C and at 900 °C. This indicates the reduction in thickness of the gate stack and/or the enhancement of the effective dielectric constant after 900 °C annealing. In contrast, the accumulation capacitances for the as-deposited and the 850 °C annealed sample did not show significant difference. Note that the gate leakage current density remains low below 10^{-8} A/cm^2 for the 900 °C annealed sample as shown in Fig. 2(d), indicating the excellent thermal stability of the Y_2O_3/GaAs interface.

To extract the correct value of dielectric constant of the oxide layers, knowing their precise thicknesses is a pre-requisite. The as-deposited oxide thickness of 16-cycle Y_2O_3 is 2.3 nm and that of 56-cycle Al_2O_3 is 5.0 nm, which have been measured/confirmed by XRR (not shown) and by STEM. Fig. 3(a) is a cross-sectional STEM micrograph, showing the as-deposited single-crystalline Y_2O_3(110) with an expected thickness of ~2.3 nm on GaAs(001). The Al_2O_3 layer did not follow the crystallinity of Y_2O_3 and was amorphous. In contrast, the bi-layered gate stack became amorphous after 900 °C annealing as shown in Fig. 3(b). Note that from the scale of the image, the total oxide thickness of the 900 °C-annealed sample remains ~7.3 nm, almost unchanged, compared to that of the as-deposited sample.

We now use the equation of $\kappa = Cd / \varepsilon_0$ to calculate the dielectric constant κ, where C is the capacitance density in μF/cm^2; d is the total oxide thickness in cm; ε_0 is the vacuum permittivity 0.885 × 10^{-7} μF/cm. With the accumulation capacitance of 1.35 μF/cm^2 measured at the probed frequency of 100 Hz, the effective dielectric constant for the as-deposited sample is ~11.1. Considering the thickness ratio of Y_2O_3 and the total oxide thickness being 2.3/7.3 ~ 0.315, the resultant dielectric constant of the total oxide film is reasonable, following Vegard's law. This result is marked as the olive round in Fig. 4. With the