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Research paper

Low-voltage DNTT-based thin-film transistors and inverters for flexible electronics

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ABSTRACT

In this article we present an integration technique for low-voltage DNTT-based TFTs for flexible electronic applications. Therefore, a high-*k* nanocomposite combining the flexibility of its polymeric matrix and the high permittivity of the incorporated inorganic material was used as gate dielectric layer. The influence of a conventional photolithography process upon the dielectric layer is analyzed regarding electrical instabilities in the device characteristics. The impact of an implemented sacrificial layer to reduce chemical stress to the insulating film during photolithography is evaluated. Furthermore, first inverter circuits were integrated and electrically characterized. Additionally, the implementation of this sacrificial layer can be used for future complementary circuit design.

1. Introduction

During the last decades several research groups and industrial companies focused their research on the development of innovative products in the field of flexible electronics. Different prototypes, such as flexible displays or smart systems responding to the devices bending state were presented and are getting close to market maturity [1–2]. Thin-film transistors (TFTs) are the primary elements of digital circuits being responsible for the current modulation in the system. In general shadow mask techniques are used to integrate their electronic connections [3–4]. Indeed, these methods provide simple and chemical stress-free fabrication processes, but large area manufacturing of energy-efficient and compact devices at low costs limits their field of application. For this technology different materials, such as metal oxides and organic compounds were evaluated as active semiconducting film [5–6]. Typical organic TFTs use SiO_2 (k ~3.9) as gate dielectric and require high operation voltages rendering them useless for portable devices (supply voltage < 5 V) [7–8]. Thus, both, photolithographic processes providing an improved integration resolution and high-k dielectrics increasing the field-induced charge carrier density at a given operation voltage are used to reduce the power consumption of the devices.

The dielectric material's surface properties play an essential role regarding the semiconductor deposition. On the one hand, a high surface roughness can create valleys in the channel region acting as traps and inhibits the growth of large and uniform crystal domains resulting in mainly polycrystalline semiconducting layers. On the other hand, the polarity of the dielectric interface has an influence either on the local morphology or on the electronic state distribution of the deposited semiconductor [9].

Admittedly, commonly used inorganic gate dielectrics, such as Al_2O_3, HfO_2 and TiO_2 provide high dielectric strength and permittivity k [10–11]. However, aiming at applications in the field of flexible electronics, the lack of flexibility (Young's modulus) limits their usage. Furthermore high temperature or vacuum processes restrict a cost-efficient integration. To overcome these issues polymeric

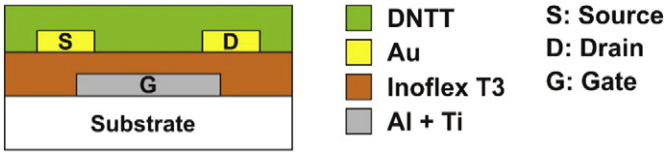

Fig. 1. Cross-section of an integrated inverted coplanar DNTT-based TFT.

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insulators are promising candidates to be employed as dielectric layer. Especially their integration capability employing solution-based methods avail the implementation to mass production processes, such as roll-to-roll techniques. Polymeric films commonly form a smooth surface, but possess low dielectric constants and weak dielectric strength [12]. Although there exist several polymers providing high *k* values as, for instance, poly(vinyl alcohol), cyanoethylated pullulan and cyanoethylated poly(vinyl alcohol) (CR-V), electrical instabilities (hysteretic behavior) could be observed due to their slowly polarized chemical species [13–15].

Another promising approach is the use of organic-inorganic nanocomposite materials. Here, the advantages of both systems, the flexibility of the polymeric matrix as well as the high *k* value of the implemented inorganic nanoparticles are combined. Nevertheless, the solid content of the nanocomposite solution affects the surface roughness of the deposited insulating film [16] resulting in a tradeoff between surface properties and dielectric constant.

Conventional photolithography becomes challenging on polymeric materials as typical developers consist of alkaline solutions. In general these chemicals damage polymer compounds by breaking their bonds leading to an increased trap density in the active insulating film.

In this article we present an integration technique for low-voltage dinaphtho[2,3-*b*:2′,3′-*f*]thieno[3,2-*b*]thiophene (DNTT) based TFTs using a high-*k* nanocomposite as the gate dielectric layer. As polymeric materials commonly suffer from alkaline solutions, the influence of a conventional photolithography process upon the dielectric layer is analyzed. To reduce the chemical stress on the dielectric during the development process, a sacrificial layer was implemented upon the insulating film. Furthermore, its influence on the device performance is evaluated. Beside the analysis of single TFTs, first inverter circuits using a control transistor in the pull-up network and a load transistor in the pull-down network were integrated and electrically characterized.

2. Integration process

In order to evaluate the influence of the chemical stress during a conventional photolithography process, two different routes for the patterning of the drain and source contacts were applied. For the first type (unprotected) the photolithography process was performed directly upon the dielectric layer. For the second protected type a sacrificial layer on top of the gate dielectric was used to minimize the chemical stress from the alkaline developer solution to the insulating film.

For both sample types the organic TFTs were integrated in an inverted coplanar setup on a Si/SiO_2 substrate acting as mechanical support (Fig. 1).

A film of 50 nm aluminum (Al) and 7 nm titanium (Ti) was evaporated under high vacuum conditions. The gate electrodes were patterned by conventional photolithography and wet etching processes using an aqueous solution of either phosphoric-, nitric- and acetic acid for the Al layer or of ammonium hydroxide and hydrogen peroxide for

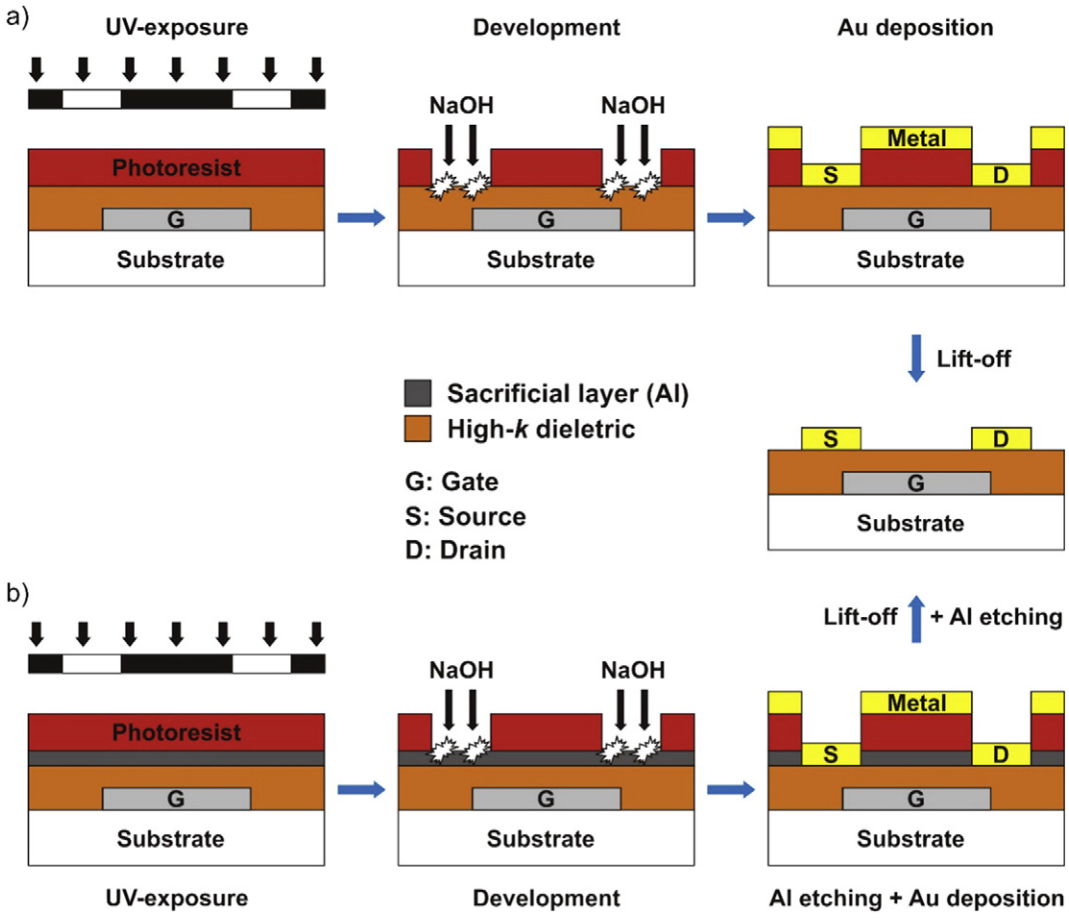

Fig. 2. a) A positive tone photoresist is applied upon the dielectric layer. The duration of the development process emerges as critical parameter as the area underneath (gate dielectric) is sensitive to alkaline solutions. b) To protect the dielectric against the used alkaline solution, a sacrificial layer is introduced before applying the positive tone photoresist. Thus, the NaOH content only affects the sacrificial layer during photolithography. Subsequent to the uncovering of the drain/source areas, the electrode material is deposited and patterned by lift-off technique. Afterwards, the residual Al is selectively removed during a wet etching step.