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Research paper

A monolithic micro-optical interferometer deep etched into fused silica

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ABSTRACT

For free-space micro-optical systems, the alignment of the components is still a challenging task in manufacturing. Alternatively, a monolithic integration can overcome this problem, but especially for in-plane optical elements in the visible wavelength range, the optical surfaces have to fulfill critical demands. Here, we show a fabrication process that allows the deep-reactive ion etching (RIE) of fused silica with high optical quality. We achieve vertical sidewalls with etch depths of about 100 μm with an arithmetic mean roughness of about 7.2 nm. By using this process, a new in-plane monolithic, free-space interferometer is demonstrated that reaches a resolution of 20 nm with our current setup.

1. Introduction

Free-space optical interferometers are commonly used for precise distance measurements. Interferometers are mostly assembled from discrete optical components such as beam splitters and mirrors on an optical bench. Therefore, it requires an individual and precise alignment of all components [1]. A single monolithic structure that includes all required optical elements would be a much better solution. Integrated interferometers using microsystems technology have already been demonstrated in silicon [2–5] and polymers [6–7]. But systems in silicon work only at infrared wavelengths, which limit the measurement accuracy as compared to the visible spectrum. Polymers have a high potential in diffractive elements [8]. But for in-plane beam guiding systems, glass still shows outstanding optical properties.

A deep silica etching process is specifically required for the presented monolithic integration. It should allow the depth of approximately 100 μm vertical sidewalls showing a roughness below sub-10 nm of the desired wavelength for high quality reflective surfaces [1]. By using other design parameter as wavelengths and light spots the requirements to the fabrication process can vary. Deep etching is already available for silicon on a commercial basis, but in silica it is much more challenging. Beyond the interferometer, deep etching of glass is targeting many applications in microfluidics, micro-optics and MEMS. Therefore, gratings [9–11], microlenses [12], microchannels [13] and piezo resonators [14] have already been realized. But nevertheless deep plasma etching of fused silica and other glasses is still challenging. The low thermal conductivity of glass requires a highly stable mask as the substrate surface heats up in the plasma despite an efficient cooling on the backside. A photoresist mask shows low selectivity and allows small etch rates and depth [15], only. In [13], an etching depth of about 100 μm was reached with mask materials such as nickel or α-Si in Pyrex-glass and fused silica. As the process is used for microfluidic applications, sidewall angle and roughness were not in focus of this process optimization. For Pyrex glass [14], a sidewall roughness of about 17 nm at an etching depth of 50 μm by using an ICP RIE process was demonstrated. Higher etching depths, which are required for free-space optical elements, have not yet been demonstrated, so far. Here, a fabrication process for deep etching of fused silica is shown, which fulfills the above mentioned requirements. By using this process, an in-plane monolithic, free-space interferometer is designed and tested.

2. Fabrication

The key technology for monolithically integrated free-space interferometers is a suitable deep silica etching process with almost vertical sidewalls and a sufficiently small roughness. This requires a highly stable etching mask with high selectivity and high-quality edges.

2.1. Substrate preparation

Electroplated nickel is a well-known material for thick etching masks up to some tens of micrometers. It is well established in MEMS-technology and therefore often used as mask material for deep glass

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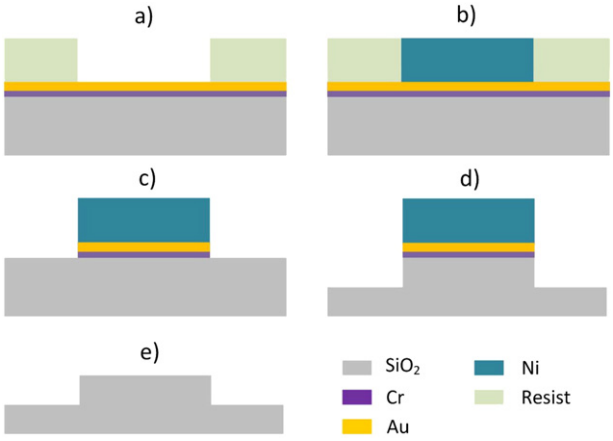

Fig. 1. Main fabrication steps: a) UV-lithography on Cr/Au-layer, b) Electroplating Ni, c) After removing resist and Cr/Au-layer, d) Deep-reactive ion etching glass, e) After removing all additional layer and plasma polymers.

etching [14,16–17]. The critical steps of the employed fabrication process are depicted in Fig. 1

Fused silica wafers with 500 µm thickness are sputter-coated with 200 nm gold on a thin chromium adhesion-promoting layer as starting layer for the electrochemical deposition of nickel. Areas to be etched later are masked by UV-lithography. It is mandatory and challenging to achieve vertical sidewalls already in the resist mask. Therefore, AZ15nXT is used as a suitable negative photoresist with the required contrast [18]. Parameters are given in Table 1. Finally, the open areas in the resist are filled with about 12 µm nickel. After removal of the resist, the remaining gold film is wet chemically removed. Therefore a commercial potassium iodide based gold etchant with additives that is compatible to nickel is used [19].

2.2. Deep etching fused silica

Etching is performed in a SENTECH Instruments Si 500 ICP-reactor (Fig. 2). The aluminum-based reactor is equipped with a turbomolecular pump for 10^{-5} Pa base pressure. The samples are fed using a loadlock. The substrate cooling is supported by a helium backside pressure of 1 kPa that enables an improved heat transfer between the sample and the electrode. The bottom-side substrate temperature is directly measured by a fiber-optic probe at the sample backside.

The tool uses a planar triple spiral antenna setup (PTSA 200) as inductively coupled plasma (ICP) source, which provides a very high ion density at low ion energy. Additionally, the energy distribution is narrow. The planar design ensures very high plasma homogeneity. An alumina plate separates reactor and ICP source. The ICP as well as the capacitively coupled plasma CCP source are driven by RF (radio frequency) generators at 13.56 MHz. The etch gases are injected into the chamber using a gas ring; the gas flow is controlled by mass flow controllers.

The etching process is fluorine based at a pressure of 0.35 Pa. Different etch gases result in different etch rates and sidewall roughness. The highest etch rate is achieved with SF_6 but the sidewall roughness is very

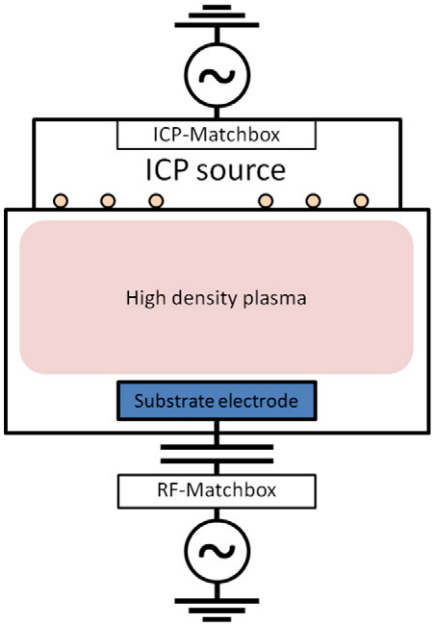

Fig. 2. Schematic drawing of the etching chamber of SI 500 with ICP and RF sources.

high. The etching process was optimized by using a combination of CHF_3 and SF_6. The overall gas flow was set to 30 sccm. By increasing the gas flow of CHF_3, the sidewall roughness decreases. Best process conditions were found at a gas ratio of CHF_3/SF_6 1:1. The optimized etching conditions are listed in Table 2. Etching rates of up to 300 nm/min have been demonstrated. The selectivity between nickel mask and fused silica was found to be 20.

The roughness of the sidewall and the etched ground was measured using a white light interferometer microscope. The arithmetic mean surface roughness (Ra) of the sidewalls was found to be as low as 7.2 nm. Fig. 3(f) shows the measured sidewall topography. The etched ground shows a Ra between 8 and 30 nm. Both are more than sufficient for micro-optical applications.

The used process shows a very small defect density over a wide etched area. In [20], different defects have been reported on the etched surfaces during the deep etching of glass. Here, a process with a high platen power of 400 W is used. Structure defects for example caused by contaminations can be reduced over a wide range, so smoothly etched surfaces can be found. Furthermore, the glass etching is dominated by the physical part of the process. An increase of physical power leads to a higher anisotropy and thus vertical sidewalls. Here, flank angles of 88° are achieved at aspect ratios of 10:1 and shown in Fig. 4. This is also suitable for microfluidic channels. Fig. 3(a–d) shows SEM images of the structures after each main process step.

Table 1
Parameters of the photolithographic process of AZ 15 nXT with vertical sidewalls.

Parameter	Value
Spin rate	750 rpm
Thickness	16 µm
Softbake	3 min @ 110 °C
Exposure dose	450 mJ/cm^2
Post exposure bake	2 min @ 120 °C
Developing	MIF 826
Remover	TechniStrip Ni555

Table 2
Process parameter for deep glass etching with optical quality.

Parameter	value
ICP power	500 W
HF(Platen) power	400 W
CHF_3	15 sccm
SF_6	15 sccm
Pressure	0.35 Pa
Temperature	20 °C
BIAS voltage	−350 V
Etch rate	300 nm/min
Selectivity (SiO_2:Ni)	20