Microelectronic Engineering 170 (2017) 34–38

Contents lists available at ScienceDirect

Microelectronic Engineering

journal homepage: www.elsevier.com/locate/mee

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# Low-cost fabrication of nanoimprint templates with tunable feature sizes at a constant pitch

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ARTICLE INFO

*Article history:*
Received 15 September 2016
Received in revised form 18 November 2016
Accepted 22 December 2016
Available online 24 December 2016

*Keywords:*
Soft UV nanoimprint lithography
NIL
Nanofabrication
Template
Cryogenic dry etching
Tunable feature sizes
Low cost
RIE
ICP

ABSTRACT

Nanoimprint lithography (NIL) templates are in general costly, especially for large area and small feature sizes. With a simple shrinking technique using a serial of well-known technologies, it has been feasibly realized to produce high-quality soft NIL templates with widely tunable feature sizes at a constant pitch from a single master at very low-cost and in a short processing cycle. The master featuring at sub-micron range has been replicated to new silicon NIL templates with feature sizes at, but not limited to, sub-200 nm. soft UV-NIL combined with a dry etch process, were employed to fabricate an intermediate template of nanocone patterns that is further used for an imprint on the final substrate. The feature size of the $SiO_2$ etch mask on the final substrate can be adjusted by varying the duration of mask formation etching. The final patterning of the template is realized by cryogenic etching based on $SF_6/O_2$ chemistry. Silicon NIL templates featuring nanopillar patterns with diameters of 150 nm, 200 nm and 250 nm, respectively, have been fabricated on wafer level from the same master with 450 nm feature size. The presented process flow avoids the time-consuming and cost-intensive electron beam writings and gives more flexibility in the fabrication of nanopatterns. The fabrication cycle for such NIL working templates with tunable feature sizes is maintained short and at a low cost. Moreover, the technique allows the fabrication of wafer level products at a constant pitch, which is of importance as well for the stacked large-area imprintings with varying feature sizes.



## 1. Motivation and overview

Nanoimprint lithography (NIL) has changed people's perception: a rather "mechanical" technique is employed for nanoscale patterning, and it caused a paradigm shift in nanolithography [1]. Utilizing a soft stamp following a lithographic scheme, the soft UV-NIL development has evolved from chip level [2] via wafer level patterning up to 300 mm substrates [3], to even ultra large patterning for meters by rolling schemes [4]. When employing soft UV-NIL, it is generally necessary to start with a master, either for replications of working soft stamps or for duplications of the template in the form of Nickel and such. The master is commonly fabricated by electron beam lithography (EBL) which is, however, costly, time-consuming and can hardly offer reasonable throughput at sufficiently high resolution [5]. Therefore, the working stamps are usually replicas from the master, nowadays in general as soft stamps replicated in PDMS or other suitable polymers.

A fast and low-cost approach to fabricate wafer-level silicon templates with tunable feature sizes for positive patterns is presented in this paper. A master featuring periodic circular pillar patterns fabricated by EBL serves as a starting point for the reproduction with tunable feature sizes. A two-step replication process is designed where the master is replicated into a cone-like patterned intermediate template and the intermediate template is employed for numerous replications of NIL template with tunable pillar diameters.

The fabrication procedure incorporates only soft UV-NIL and subsequent dry etch processes. The processes involve no further electron beam writing for patterning, which therefore leads to a low cost and fast acquisition of NIL templates. The feature size (and shape) of the new set of templates can be effortlessly adjusted during the respective etch process, which was one of the key motivations of this work. Moreover, the process is designed also based on the fact that, for certain applications, it is critical to imprint varying feature sizes at identical pitch on the same substrate at different stages of fabrications. In 1D surfaces, such as applications of graded index photonic crystals or anodic aluminum oxide membranes, the radius of the patterns is in graded or stepped manner whereas the pitch size is maintained [6,7]. In multi-stack alignment, the pitches of the multiple layers are commonly kept constant while within each layer the feature size can vary if necessarily designed [8]. Therefore, the template series generated from one and the same master is of great importance to avoid variations in pitch or device alignment.

The theoretical methodology of the fabrications is demonstrated in next section and the corresponding experimental results will follow.

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http://dx.doi.org/10.1016/j.mee.2016.12.023
0167-9317/

## 2. Methodology

A schematic process flow of the template fabrication is depicted in Table 1. A master is fabricated by EBL and its surface is coated with an anti-sticking layer (Step A). A soft stamp made of UV-curable PDMS is replicated from the master (Step B) and used for the first imprinting (Step C). An intermediate silicon template featuring cone patterns is etched (Step D) and applied for further soft stamp replications (Step E). A silicon substrate featuring a hard mask layer is imprinted using the soft stamp, thus transferring the cone patterns in the UV-NIL resist (Step F). The feature size of the final template is determined by the diameters of the etch mask, respectively. By exposing the substrate to variable etch durations, the hard mask is opened according to the slope of the cone pattern (Steps G-1/G-2/G-3 for comparison). Taking the resulting non-vertical profile of the hard mask into account, cryogenic silicon etching based on $SF_6/O_2$ chemistry is employed to etch the silicon substrate. It offers a fast etching of silicon with smooth and vertical sidewalls at high selectivity with respect to the mask. Afterwards the mask is completely removed (Steps H-1/H-2/H-3). The detailed process parameters and materials used are explained in the subsequent section.

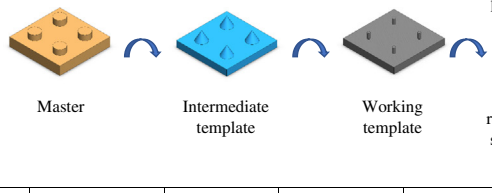
## 3. Results and discussion

A nanopillar array of 5 cm × 5 cm centered on a 150 mm silicon wafer is used as the master. The nanopillars have a diameter of 450 nm at a pitch of 1000 nm and a height of 700 nm. Scanning electron microscope (SEM) images of the master are displayed in Fig. 1a (cf. Step A).

A monolayer of Perfluorodecyltrichlorosilane (FDTS) was deposited onto the surface of the master due to its excellent anti-sticking properties in vapor phase at 165 °C within 2 h. The soft UV-NIL system (GD-N-03, GDnano Ltd.) employs a center-to-edge stamp bowing scheme [5, 12] for imprinting on the 100 mm silicon wafer with a low back pressure below 0.5 kPa. A bi-layer soft stamp is established for imprinting. The stamp consists of a 2 mm thick PDMS carrier and a 500 μm feature layer made of UV-PDMS (Shin-Etsu). The UV-PDMS features a 0.02% shrinkage enabling a high replication fidelity of the master patterns [13]. The PDMS carrier was produced at a mixing ratio of 10:1 (base:curing agent) by weight and cured separately in advance. The UV-PDMS, which is originally served as two component product, was mixed at a ratio of 1:1 (base:curing agent) and dispensed on the FDTS-treated master. The UV-PDMS was co-cured on the PDMS carrier by UV exposure at 365 nm at a dose of at least 2000 mJ $cm^{-2}$ and post-cured for 3 h at room temperature before peeling off from the master to reach the required physical properties (Fig. 1b).

The resist used for the first imprinting of intermediate template is AMONIL MMS4 (AMO GmbH). It is non-sensitive to oxygen and PDMS-compatible, thus meeting the requirement of nanoimprint lithography in ambient atmosphere. The resist was spin-coated at 4000 rpm for 1 min, resulting in a height of approximate 700 nm and a residual layer thickness of less than 50 nm. The imprinted wafer is shown in Fig. 2a. The residual layer is descummed by means of reactive ion etching (RIE) utilizing a gas combination of $CHF_3$ and Ar afterwards (cf. Step C). Employing the patterned resist as mask, the silicon substrate is undercut into cone-like structures by plasma etching in $SF_6$ and $O_2$. The etched patterns are shown in Fig. 2b (cf. Step D). The PDMS/UV-PDMS bi-layer soft stamp was then replicated from the intermediate silicon template which has been coated with FDTS as well. The dimension, i.e. the volume, of the cone patterns decreases compared to the pillar patterns. Therefore, the coating thickness of the resist is preferably reduced in order to achieve a possibly thin residual layer after the imprinting. The AMONIL was diluted by Isopropoxyethanol at a ratio of 1:1 by weight owing to its lower evaporation rate in comparison to that of ethanol. The silicon substrates as for the final NIL templates are thermally oxidized for 50 nm $SiO_2$ layer as hard etch mask. On one hand, resist faces high risks of cracking at cryogenic temperature which is

**Table 1**
Schematic process flow of the template fabrication with tunable feature sizes for nanopillar patterns.




| Step | 3D–view | Top view | Side view | Description |
|---|---|---|---|---|
| A | | | | NIL master fabricated by EBL. Surface treatment with FDTS (anti–sticking layer). |
| B | | | | Soft stamp replication from the master. Stamp consisting of PDMS carrier and UV–PDMS feature layer. |
| C | | | | First imprinting and descumming of the residual resist layer. |
| D | | | | Dry etching of nanocone pattern on the intermediate template. |
| E | | | | PDMS/UV–PDMS soft stamp replicated from the intermediate template. |
| F | | | | Second imprinting on the silicon subtrate featuring a hard silicon dioxide mask on top. |
| G–1 | | | | Residual resist descumming and hard mask etching (short duration). |
| H–1 | | | | Cryogenic silicon etching for the final NILworking template (mask removed). Short mask etch duration = large pillar diameter. |
| G–2 | | | | Residual resist descumming and hard mask etching (medium duration). |
| H–2 | | | | Cryogenic silicon etching for the final NIL working template (mask removed). Medium mask etch duration = medium pillar diameter. |
| G–3 | | | | Residual resist descumming and hard mask etching (long duration). |
| H–3 | | | | Cryogenic silicon etching for the final NIL working template (mask removed). Long mask etch duration = small pillar diameter. |