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Research paper

# Impact of gold deposition parameters on the drain-source leakage current in top-contact pentacene-based thin-film transistors

Wenjie Qin *, Holger Goebel

*Department of Electronics, Helmut Schmidt University/University of the Federal Armed Forces, Holstenhofweg 85, D-22043 Hamburg, Germany*

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ABSTRACT

In this work the influence of gold deposition parameters such as substrate temperature and nominal contact thickness on the drain-source leakage current in top-contact pentacene-based thin-film transistors (TFTs) is investigated. The results reveal that the drain-source leakage current can be suppressed by increasing the substrate temperature and by decreasing the gold contact thickness. It is shown that the observed behavior cannot be fully explained by the standard leakage current model, which attributes the decrease of the leakage current to an increase of the contact resistance. Therefore an extended leakage current model is introduced which takes into account the so-called halo-effect, i.e. the formation of a layer of gold clusters during the gold diffusion process, yielding a parallel resistance between drain and source. It is shown that this model is able to describe both, the dependency of the leakage current on the substrate temperature as well as on the contact thickness.



## 1. Introduction

Organic thin-film transistors (OTFTs) are of growing interest because they allow the fabrication of innovative devices such as conformable sensor arrays and flexible active-matrix displays that might be difficult to achieve by utilizing conventional silicon technologies [1,2]. In the last two decades, progress in organic electronics has been accomplished primarily by improvement of the mobility of organic semiconductors, increase in the capacitance of suitable gate dielectrics, and reduction of the key dimensions of the devices. Size reduction, in particular, represents a powerful approach for transistors to obtain high current capability and switching speed. However, the contact resistance between the organic semiconductor and the source and drain electrode, respectively, becomes increasingly crucial to device performance as the channel length decreases. Although top-contact configuration can be utilized to reduce the relative contribution of the contact resistance to the total device resistance [3], an undesirable increase of the so-called anomalous drain-source leakage current has often been reported for both long-channel [4] and short-channel top-contact OTFTs [5–8]. Recently, we have also reported that for top-contact pentacene based TFTs with channel lengths of 30 μm, the drain-source leakage current with an ohmic behavior was found to increase with increasing the gold deposition rate, which can be explained based on a physical model in which the gold clusters diffuse laterally from drain-source edges into the channel region underneath the standard shadow mask during gold deposition, leading to a leakage resistance in parallel with the pentacene thin film [9]. Although the dependence of the drain-source leakage current on the gold deposition rate was discussed in our previous work [9], the influence of other gold deposition parameters on the drain-source leakage current has not yet been investigated.

In this work we therefore study the influence of the substrate temperature ($T_{Au}$) during gold deposition and the gold contact thickness ($t_{Au}$) on the drain-source leakage current ($I_{L,DS}$) in top-contact pentacene-based thin-film transistors with channel length (L) of 20 μm. Since in the standard model for the anomalous leakage current [4,6] the decrease of the current is attributed to the increase of the contact resistance, we also provide an analysis of the relationship between leakage current and contact resistance ($R_C$) with respect to different deposition parameters ($T_{Au}$ and $t_{Au}$) in order to examine whether the standard model can be used to explain our measurement results. At the end of this work, by using the physical model referred in our recent work [9] instead of the standard model, the dependence of the leakage current and contact resistance on both the substrate temperature and the gold contact thickness is successfully explained.

## 2. Device fabrication

Top-contact pentacene TFTs as shown in Fig. 1(a) were fabricated on an arsenic-doped silicon wafer (resistivity = 0.001–0.005 Ω cm) with a 300-nm-thick silicon dioxide ($SiO_2$), which forms the gate and the dielectric layer, respectively. Prior to the pentacene film deposition, substrates cut from the same wafer with $SiO_2$ dielectric layer were rinsed with acetone and isopropanol sequentially in an ultrasonic bath for 10 min each, and then were wet cleaned with deionized water, blown

* Corresponding author.
*E-mail address:* qinw@hsu-hamburg.de (W. Qin).

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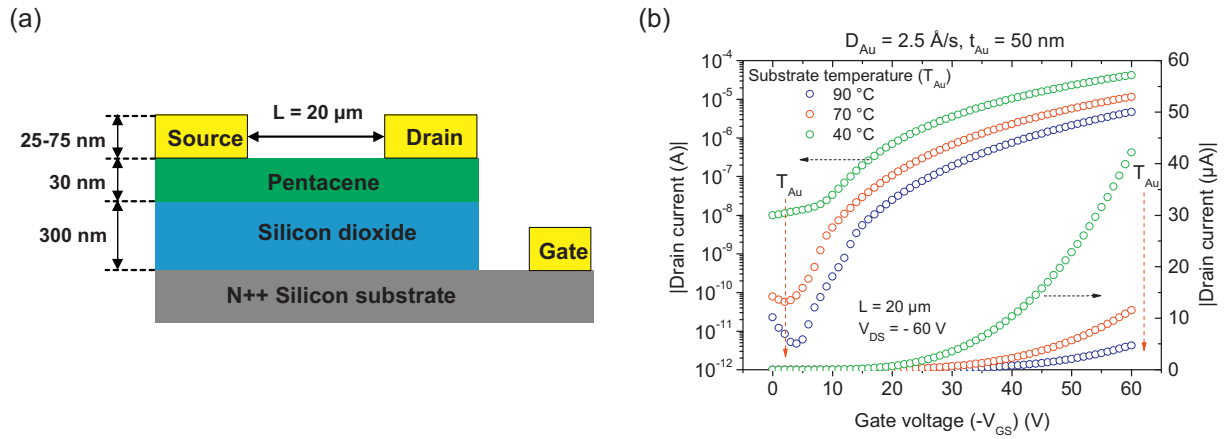


**Fig. 1.** (a) Schematic drawing of the manufactured top-contact pentacene TFT (cross-section). (b) Measured transfer characteristics of the top-contact pentacene TFTs (L = 20 µm, $D_{Au}$ = 2.5 Å/s, $t_{Au}$ = 50 nm) fabricated with different $T_{Au}$ in the range from 40 °C to 90 °C.

with a nitrogen gun, and heated at 120 °C for 1 h in a dry nitrogen atmosphere.

Based on these substrates we fabricated two sets of transistors in a glove box (*MBraun*) with $O_2$ and $H_2O < 0.1$ ppm. The first set (Set I) was used to investigate the influence of $T_{Au}$ on $I_{L,DS}$. For the preparation of Set I, a 30-nm-thick layer of pentacene (sublimed grade and purity = 99.9%) purchased from Sigma-Aldrich was thermally evaporated onto the substrates at a rate of 0.50 Å/s in a vacuum chamber at about $10^{-6}$ mbar to form the active layer. Based on the different $T_{Au}$ in the range from 40 °C to 90 °C, a 50-nm-thick gold (Au) contact layer was then sequentially deposited onto the active layer by thermal evaporation through a hard-electroformed-nickel-based shadow mask to define the transistors with the channel width of W = 1 mm and the channel length of L = 20 µm. The deposition rate for the creation of the gold contacts was maintained at 2.5 Å/s. A second set (Set II) of transistors was prepared to further investigate how $t_{Au}$ affects $I_{L,DS}$ and $R_C$. For the fabrication of Set II, gold contact layers with different thicknesses (25, 50, 75 nm) were sequentially deposited at a rate of 1.0 Å/s on the pentacene layers that were fabricated with the same parameters as in Set I through a shadow mask to define five transistors with the same W = 1 mm and L in the range of 20–70 µm. The substrate temperature during the gold deposition was maintained at room temperature (25 °C) using a water-cooling system. All electrical measurements of the pentacene TFTs were performed using an Agilent 4156C semiconductor parameter analyzer in the glove box in a dark environment.

## 3. Results and discussion

### 3.1. Influence of $T_{Au}$ on $I_{L,DS}$

In Fig. 1(b), the measured transfer characteristics for pentacene TFTs with different $T_{Au}$ from Set I are shown. It can be seen that both, drain-source current in the off-state ($I_{L,DS}$) and drain-source current ($I_{On,DS}$) in the on-state ($V_{GS} = -60$ V) decrease with increasing $T_{Au}$. These results suggest that the behavior of the leakage current can be explained by the variation of the contact resistance $R_C$ as mentioned in Ref. [4,6] where it was shown that for top-contact pentacene TFTs the drain-source leakage current can be significantly suppressed using a high-resistive contact region. This model, hereafter referred to as the standard model, is based on the assumption, that the leakage current uses a conducting path from the source into the bulk material, i.e. the pentacene, and from there to the drain. As a physical explanation for this behavior, it was reported that with a higher $T_{Au}$ more gold atoms tend to diffuse into the pentacene layer, which can perturb the stacking geometry of the pentacene molecules in the contact region, and thus increase the injection barrier height at the drain-channel junction, causing an increased $R_C$ [10]. Therefore, it is rational to deduce that in the presented case the observed decrease of the drain-source current in the off-state as well as in the on-state might originate from the increase of the $R_C$ at the contact region induced by a high $T_{Au}$.

### 3.2. Influence of $t_{Au}$ on $I_{L,DS}$ and $R_C$

To get a deeper understanding of the physical mechanisms underlying the leakage current, we also investigated the relationship between the contact thickness $t_{Au}$ and the contact resistance $R_C$ of OTFTs [11,12]. For that purpose we used transistors with different contact thicknesses (Set II) and measured the relationship between $t_{Au}$ and $I_{L,DS}$ and $R_C$. The measured transfer characteristics for pentacene TFTs (L = 20 µm) with different $t_{Au}$ are shown in Fig. 2(a). It can be seen that $I_{L,DS}$ increases with increasing $t_{Au}$ whereas $I_{On,DS}$ decreases with increasing $t_{Au}$. In order to correlate these results with the contact resistance $R_C$, we used the same measurements to estimate the contact resistance $R_C$ for different $t_{Au}$. According to the transfer line method (TLM) [13] the total on-resistance of the transistor in the linear region ($R_{total}$) is given by the standard equation

$$R_{total} = R_{ch} + R_C = \frac{L}{WC_{OX}(V_{GS} - V_{TH})\mu_{ch}} + R_C, \quad (1)$$

where $R_{ch}$ and $\mu_{ch}$ are the channel resistance and channel mobility, $C_{OX}$ is the insulator capacitor per unit area, and $V_{TH}$ is the threshold voltage. The values of $R_{total}$ normalized with respect to the channel width W of the TFTs with different $t_{Au}$ are plotted as a function of L in Fig. 2(b). The values of $R_C$ can then be obtained from the *y* intercepts. The change of the W-normalized contact resistance with varying $V_{GS}$ [Fig. 2(c)] reveals that $R_C$ increases as $t_{Au}$ increases. In addition, the W-normalized channel resistance ($R_{ch}$) with varying $V_{GS}$ based on different $t_{Au}$ is shown in Fig. 2(d). The most important results are summarized in Table 1 showing the numerical values of the leakage current, the on-current, and the channel width-normalized resistance for transistors with different contact thicknesses. First, it can be seen that increasing $t_{Au}$ (and thus increasing $R_C$) yields a reduction of $I_{On,DS}$ (Fig. 2(a)), as expected. At the same time, however, the increase of $t_{Au}$ (and thus increasing $R_C$) causes the leakage current $I_{L,DS}$ to increase, which contradicts the above-mentioned assumption of the standard model. Therefore we conclude that the source-bulk-drain leakage path of the standard model cannot be the only source for the observed leakage current. Instead, we propose an extended leakage current model as explained in the following section.