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Research paper

Edge trimming for surface activated dielectric bonded wafers

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ABSTRACT

The impact of the edge trimming process on permanently bonded wafers is described. The edge trimming process is a blade sawing process applied on the Si wafer edge and bevel, removing the fragile edge of the wafer prior to grinding. We investigated two routes for the integration on permanently bonded Si wafers, edge-trim before bonding and edge-trim after bonding. The impact on the subsequent processes for both integration routes is assessed. For the case of edge-trim before bonding, a combination of functional water cleaning such as ozone dissolved in water and ammoniac scrub cleaning shows a significant effect to remove Si residues, enabling void free dielectric bonding. For the case of edge-trim after bonding, utilizing a small grit diamond blade shows no mechanical failures into the dielectric bonding interface. These proposed processes are a very promising for the fabrication of extreme thinned Si without mechanical failure at wafer edge.

1. Introduction

3D integration has developed utilizing vertical through-Si vias (TSV) and bumping connections [1–3]. Nevertheless, due to the thin wafer handling and stacking issues, there is a limitation of minimum Si thickness, corresponding scaling of TSV dimensions and pitches. Recently, wafer-to-wafer 3D stacking by using dielectric [4–6], polymer [7,8] and hybrid [9–11] bonding are getting more and more attention. The wafer-to-wafer 3D stacking potentially offers a solution for thin wafer handling issues allowing the removal of most of the Si from the top wafer. Extremely thin Si (<5 μm) can extend the scaling of TSV interconnections. The TSV formation is significantly influenced by the thinning performance, which brings new challenges in the thinning process. One of the challenges of the thinning step is to avoid mechanical failures. The most fragile part during the Si thinning is the wafer edge [12–14], with a knife edge shape after grinding. Fig. 1 shows the schematic illustration of post grinded dielectric bonded wafers without any edge preparation prior to grinding. The knife shape edge can appear on the top wafer edge. Fig. 2(a) shows the actual result after grinding of permanent bonded wafer without edge preparation. The sharp edge will easily cause chipping and delamination, as shown in Fig. 2(b) which is a top view optical microscope (OM) picture at the wafer edge. In addition, the broken Si piece might create a lot of particles on the surface and the bevel.

In order to remove the knife edge shape, an abrasive sawing process by using a mechanical diamond blade (so called edge trimming) is a promising process to remove the wafer edge prior to grinding [13,14]. During this process, the wafer is turned with cutting of the top edge by a high speed spinning diamond blade. Although edge trimming is based on a conventional diamond blade dicing technique, the impact on the wafer bonding process has not sufficiently been investigated.

In this paper, we investigated the edge trimming process for dielectric bonded wafers. The impact on the subsequent process for both integration routes, edge-trim before bonding (Fig. 3(a)) and edge-trim after bonding (Fig. 3(b)).

2. Experimental

The edge trimming process was performed by using the dicing saw tool DFD6860HC from Disco. All the tests were done on 300 mm Si wafers (775 μm thickness). The trimming width is fixed at 500 μm from the wafer bevel edge. The blade spindle speed was 30,000 rpm and the feed rate of the wafer (turning speed of the chuck table) was 5°/s. 1 mm width blades were used. The grit size of the edge-trim before bonding is #1500. The height were 150 or 250 μm for performing edge-trim before bonding. The force during edge trimming process was monitored by current of spindle motor. The motor current during idle running with 30,000 rpm is around 0.5 A. Post edge trimming cleaning is done in an in-situ cleaning unit of the tool. Atomizing deionized water (DIW) cleaning (800 rpm for 60 s) and spin drying (1500 rpm for 35 s) were used for rinsing and drying unless otherwise specified. Furthermore, dissolved ozone (O_3; 20 ppm) into DIW as functionalized

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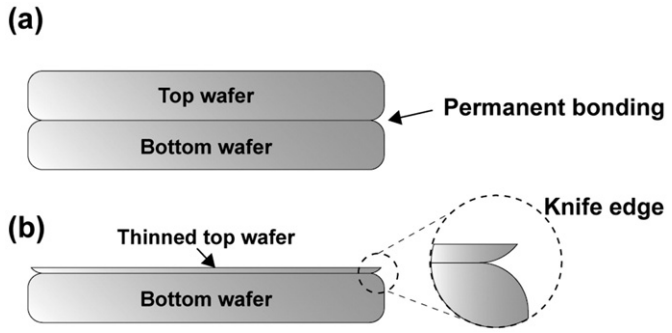

Fig. 1. Schematic images of dielectric bonding without edge trimming (a) post dielectric bonding (b) post grinding.

water and ammonia hydroxide (0.016 mol/L) were dispensed from a nozzle on wafer surface. Scrub cleaning is done by a pencil type of polyvinyl alcohol (PVA) sponge with liner movement at a certain height. For the case of edge-trim after bonding, different blades were tested (#400, #1000 and #1500). The depth for the case of edge-trim after bonding is 825 or 925 μm to reach the cut into the carrier wafer. The spindle current and blade wear are measured in-situ.

The permanent wafer bonding was performed before or after edge-trim process by using plasma activated dielectric bonding. The dielectric layer (SiOx) was deposited by plasma enhanced chemical vapor deposition (PECVD). The PECVD layers were deposited with a certain temperature as low as 370 °C. Sequentially, the thermal anneal of 20 min at the 420 °C was performed to densify the film. Chemical mechanical polishing of the surface dielectric layer is used to planarize and to smoothen the dielectric layer. The RMS of the dielectric surface was below 0.3 nm after CMP. Prior to bonding, the pairing wafers are treated by N_2 plasma activation. Wafer bonding takes place at room temperature in an atmospheric pressure in a clean room ambient followed by an annealing at 250 °C for 2 h to improve the interfacial adhesion strength. The obtained bonding strength after annealing, measured by double cantilever beam test, was above 2.0 J/m^2 as mean value. The cross-sectional images were obtained by scanning electron microscopy (SEM; FEI Nova NanoSEM200). The defect inspection was done a KLA-Tencor SP2. The interfacial spacing was obtained by Scanning Acoustic Microscope (SAM; PVA Tepla SAM300 Auto Wafer).

3. Results and discussion

3.1. Edge-trim before bonding

Fig. 3(a) shows the process flow of edge-trim before dielectric bonding. This process is a single wafer process, with edge cutting from the front side. As the edge trimming process is applied before bonding, no particles (dicing shaving) should remain on the surface. Otherwise the particles will be entrapped into the wafer to wafer interface during bonding. The entrapped particle will make a void at the interface, which will have a huge impact on subsequent processing. Fig. 4 shows cross-sectional SEM images after edge trimming on a single wafer. In

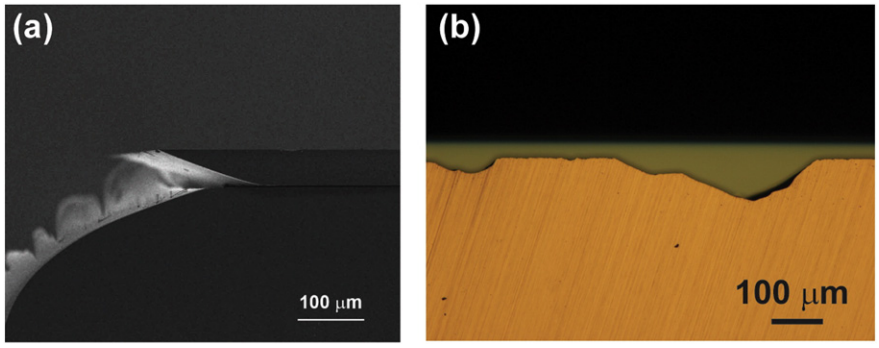

Fig. 2. (a) Cross-sectional SEM image of bonded wafer edge after top wafer grinding towards 50 μm thickness without edge trimming (b) Top OM view of wafer edge after grinding without edge trimming.

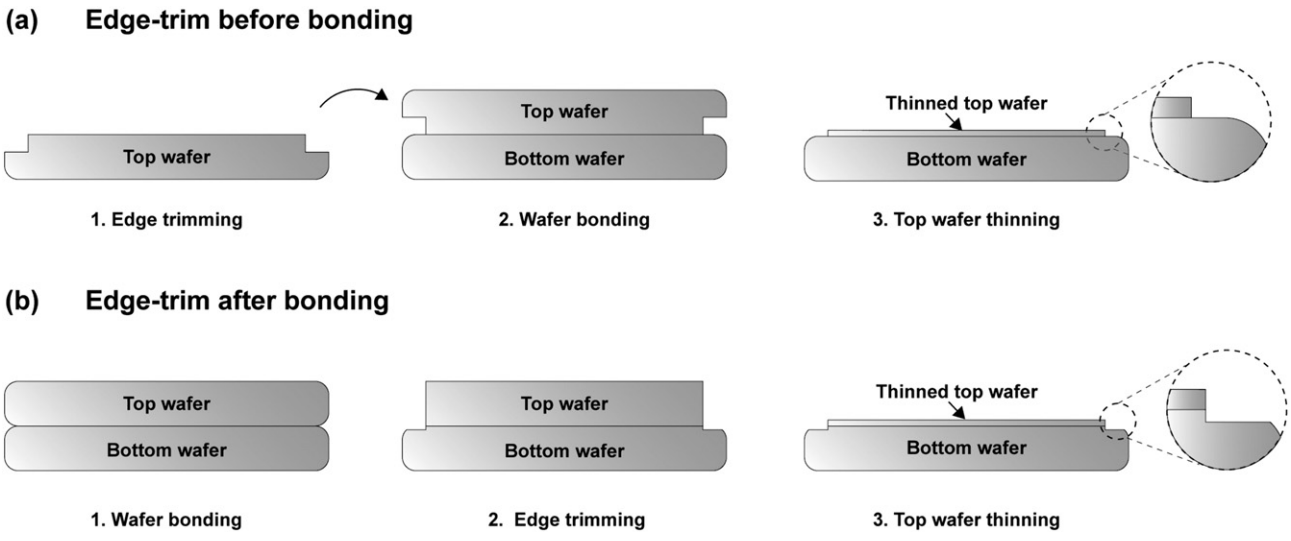

Fig. 3. Schematic illustration of edge trimming process flow (a) Edge-trim before bonding (b) Edge-trim after bonding.