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Research paper

Behavior of copper contamination on backside damage for ultra-thin silicon three dimensional stacking structure

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A B S T R A C T

Bumpless interconnects and ultra-thinning of 300 mm wafers for three-dimensional stacking technology have been studied. In our previous work, thinning effects using device wafers <10 μm thick were reported. No degradation occurred in the retention time even in a 4-μm-thick DRAM wafer. In this study, the behavior of Cu contamination on a <3-μm-thick DRAM wafer was investigated. The wafer was thinned down by coarse (#320 grit size) grinding and fine (#2000 grit size) grinding. This thinning condition had 200-nm-thick ground damage remaining for the gettering effect. The DRAM wafer was intentionally contaminated with Cu on the damaged layer, and 250 °C-60 min of heating was carried out during adhesive bonding and de-bonding. Degradation in the device characteristics was found. However, the analytical results indicated that the Cu did not diffuse into the thin Si. Thus, a Cu contaminated blanket wafers having a damaged layer were prepared and annealed until 1000 °C-30 min. Secondary ion mass spectroscopy, transmission electron microscopy and positron annihilation spectroscopy were evaluated. The Cu was trapped in the vacancy-type defects of the 200 nm damaged layer until a 700 °C anneal. After an 800 °C anneal, the Cu was eliminated on the damaged surface because of the Si recrystallization. The gettering ability of the damaged layer is suitable for 3D multi-level stacking regarding thermal stability.
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1. Introduction

Bumpless interconnects and ultra-thinning of 300 mm wafers for three-dimensional (3D) stacking technology have been studied [1,2]. The merits of wafer-on-wafer (WOW) stacking technology are that it is superior in mass production and that the front end wafer process compatibility enables the 3D stacking process to be handled within wafer fabrication plant. Fig. 1(a) shows the advantages of an ultra-thinned 3D structure. 50-μm Si die and 30-μm bumps are assumed for the conventional process. If bumps are eliminated, the limitation on Si thickness can be decreased because the mechanical strength is mitigated. Thus, we designed ultra-thin 5 μm Si, reduced the form factor to one-20th, and increased the number of TSVs to 1 billion. Fig. 1(b) explains the advantages of the thinned Si and small TSV structure. Thin Si provides low aspect ratio TSVs. Shortening the wiring length provides RC delay mitigation. Also, high IO density accomplishes the low frequency and high bandwidth needed to reduce the power consumption. To enable all of these benefits, we developed bumpless ultra-thin stacking technology [3–5].

In our previous studies, the wafer thinning effect using device wafers <10 μm-thick was investigated [6,7]. No change occurred in the retention time before and after thinning even in a 4-μm-thick DRAM wafer [8]. In the meanwhile, many studies on Cu contamination for the Si wafer have been reported because Cu contamination for the transistors degrades device characteristics [9–12]. Therefore, we evaluated a DRAM wafer <10 μm thick with a Cu contaminated structure [13]. DRAM characteristics were examined using different Si thicknesses including with and without Cu contamination. In the 5.5-μm-thick 300 mm wafers, no changes occurred in the retention time before and after thinning even with the Cu contamination wafer. However, on the 2.6-μm-thick wafers, degradations were observed even without a Cu contamination wafer (Fig. 2). All wafers were ground by #2000 grit abrasive. These results indicate that the thickness is dominant compared with Cu contamination for the device degradation.

The issue of a thinner Si structure is our primary concern. Fig. 3 explains the gettering ability of a Si wafer. Conventionally, a Si wafer is composed of a defect-free zone and an intrinsic gettering layer [14,15]. The thickness of a denuded zone is approximately 3–10 μm. If the wafer backside is attacked by impurities, the gettering layer can catch

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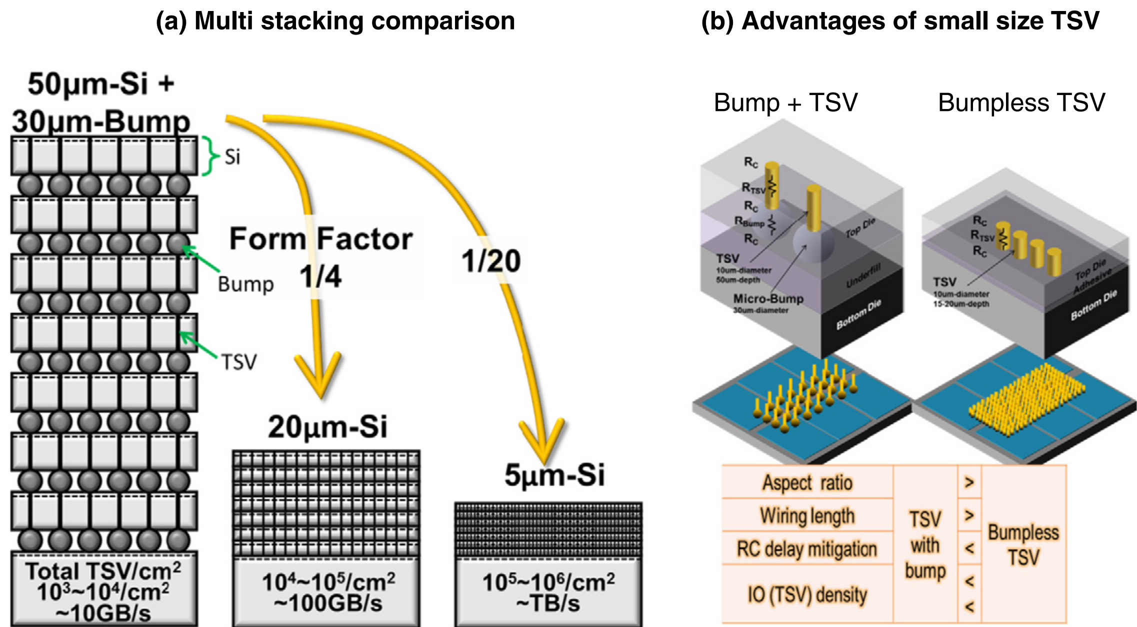

Fig. 1. Advantages of ultra-thinned 3D structure. (a) Multi-stacking comparison between conventional 3D stacking structure and bumpless ultra-thin Si stacking structure. (b) Advantages of the thinned Si and small size TSV structure.

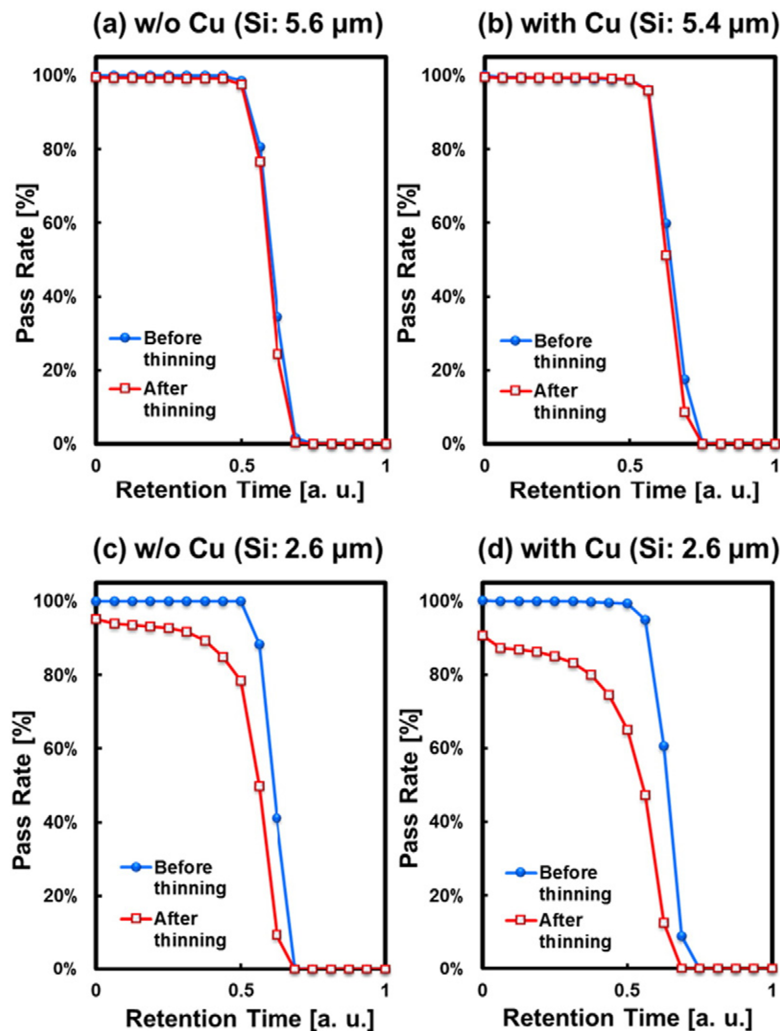

Fig. 2. DRAM yield as a function of retention time for (a) as-formed (Si = 5.6-µm), (b) with Cu contamination at the backside of wafer (Si = 5.4-µm), (c) as-formed (Si = 2.6-µm) and (d) with Cu contamination at the backside of wafer (Si = 2.6-µm). All wafers were ground by #2000 grit abrasive.

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