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Research paper

Fabrication of self-aligned multilevel nanostructures

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ABSTRACT

Multilevel three-dimensional nanostructures are essential in many integrated nanoelectronic and nanophotonic applications. With the continued shrinking of critical device dimensions, extremely precise nanoscale overlay is required between multiple individual levels of these integrated devices. Multilevel nanoimprint lithography has been proposed in the literature as a potential solution to this overlay problem. In this context, self-aligned (perfectly aligned) multilevel templates (SAMT) for multilevel nanoimprint lithography are proposed in this article. By combining nanolithography, atomic layer deposition, and highly selective reactive ion etch, SAMTs can enable the fabrication of sophisticated integrated devices. Four specific self-aligned multilevel fabrication techniques have been demonstrated that result in symmetric multilevel structures, bilaterally symmetric multilevel structures, tubular structures, and asymmetric multilevel structures, all in the sub-100 nm scale. When used in conjunction with a nanoimprint lithography process, the SAMTs can enable high-throughput patterning of various nanoelectronic and nanophotonic devices using a single patterning step with perfect alignment and overlay. SAMTs further enable large area patterning, such as wafer-scale patterning and roll-to-roll patterning on flexible substrates, without compromising perfect overlay.

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1. Introduction

As critical device dimensions continue to scale aggressively in keeping with Moore's Law, fundamental limits to feature resolution are being reached for several state-of-the-art top-down nanopatterning techniques, thus constraining the performance as well as the packing density of the devices. For example, a typical 193 nm immersion (193i nm) optical lithography process has an ultimate achievable imaging resolution of ~36 nm [1]. For some of the most advanced devices in nanoelectronics that have feature dimensions smaller than this limit [2], several techniques, such as double patterning, optical proximity correction, and phase shift masks have been used. These result in significant increase in cost due to the greater number of subsequent non-lithographic process steps [3–5]. At the same time, directed self-assembly (DSA) techniques are being explored to complement 193i nm lithography, especially for via hole shrink applications [5–10]. However, these techniques are limited to periodic patterns and have problems with long-range order. Likewise, significant challenges remain with electron beam [11] based techniques, such as multiple e-beam lithography (MEBL), and other higher resolution photon beam based techniques, such as extreme ultraviolet lithography (EUVL) [12–15].

Also, all the above techniques have been developed for patterning substantially planar layouts on the surface of a rigid substrate. They cannot be directly translated to nanoscale patterning on non-traditional substrate configurations, such as flexible substrates in a roll-to-roll format or across entire wafers beyond a smaller patterning field. They are also typically unable to pattern non-planar, three-dimensional structures in a single step. These structures are being explored to overcome fabrication complexity, packing density and performance constraints of standard surface-patterned devices. For example, three-dimensional FinFETs have been demonstrated to have highly desirable properties while not compromising with packing density constraints [16–18]. Similarly, three-dimensional photonic crystals allow for enhanced functional characteristics compared to traditional two-dimensional designs [19]. However, their fabrication requires that each level in such multilevel three-dimensional devices, is patterned individually, thus placing extremely stringent constraints on level-to-level alignment.

In this regard, nanoimprint lithography [20–24] has been demonstrated as a high throughput, low-cost lithographic technique capable of patterning arbitrary geometries with demonstrated sub-10 nm feature resolution. Moreover, multilevel imprint lithography has been demonstrated to pattern multilevel structures with high-fidelity by replicating an existing multilevel pattern on the template [25–28]. Since the multilevel pattern is pre-coded in the template geometry, multilevel imprint lithography can lend itself to faithful and cost-effective replication of the same geometry without needing further alignment or overlay. But, such demonstrations have only been carried out with micron-

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scale resolution. Hence, the goal of this work, is to enable multilevel imprint lithography with nanoscale resolution and perfect alignment between individual levels.

2. Motivation

One of the challenges associated with fabrication of multilevel three-dimensional structures with traditional patterning techniques is the need for precise level-to-level alignment. Misalignment gives rise to the problem of nanoscale overlay, which refers to the accuracy with which a patterned field can be registered relative to a previously lithographed field. Overlay requirement is typically one-half to one-quarter of the minimum feature size [23], which can be extremely tight for features in the sub-20 nm regime. The current best achievable overlay with nanoimprint lithography is 10 nm (mean + 3σ) over a field size of 26 mm × 33 mm [29]. This problem of overlay is exacerbated when imprinting on flexible substrates, that have significant distortion, or over extremely large areas in a single step on rigid substrates [30]. With multilevel nanoimprint lithography using a template with nanoscale features, this can be overcome. However, the nanoimprint template now needs to be fabricated with precise level-to-level alignment over large areas. In previous demonstrations of multilevel imprint lithography [25–28,31–39], individual levels on the imprint template were fabricated using multiple optical or electron beam lithography steps. This limits the best possible overlay that can be achieved between consecutive levels due to inherent tool limitations. Overcoming this overlay constraint by fabricating self-aligned multilevel nanoimprint lithography templates (SAMTs) is the key motivation behind this work. The methodology for fabrication of SAMTs is described in Section 3.

For validation of the benefits of perfect level-level alignment, three exemplar devices have been identified. The first device relates to a NMOS transistor array, which can be patterned in a single step across large areas if a SAMT is used. The optimum geometry for such a SAMT is shown in Fig. 1(a). The process of using this SAMT to fabricate wafer-scale NMOS arrays is discussed in Appendix A [40]. This SAMT can in turn, be fabricated using a bilaterally symmetric multilevel geometry highlighted by the red rectangle and illustrated in Fig. 1(b) [28,40]. A self-aligned process to fabricate such bilaterally symmetric multilevel structures (Fig. 1(b)) is demonstrated in Section 4.

The second exemplar device is a nanotube capacitor, for which the geometry is shown in Fig. 2. In previous work [41,42], it has been shown that the performance of nanoscale capacitors depends on the surface area. With the use of multilevel patterning and perfect alignment, solid circular cross-sections of these capacitors can be enhanced into hollow tubular cross-sections. This increases the surface area dramatically, thereby increasing the unit capacitance of such devices [43]. Demonstration of self-aligned Si tube structures is discussed in Section 5.

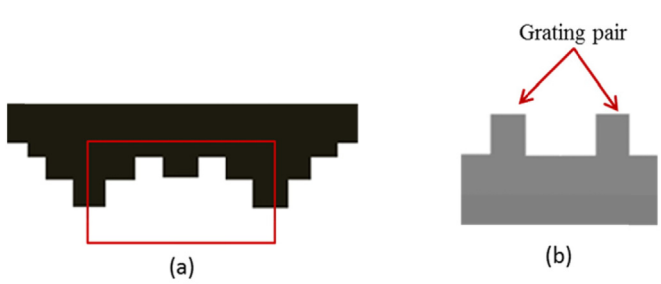

Fig. 1. Illustration of (a) nanoimprint replica template for fabrication of NMOS arrays on a wafer-scale (b) bilaterally symmetric multilevel structure on master template highlighting the geometry within the red rectangle in (a). (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

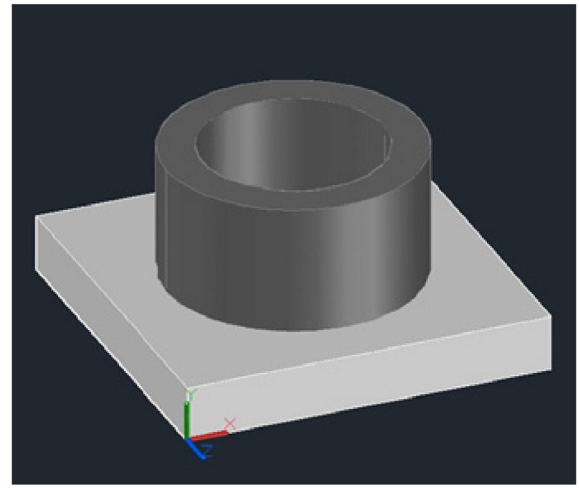

Fig. 2. Illustration of self-aligned Si tubes for fabrication Si tube capacitors.

The third device that can benefit from multilevel imprinting is a metamaterial wire-grid polarizer (WGP). Through modeling using the finite difference time domain (FDTD) technique and geometric optimization using genetic algorithms [40], it can be observed that the use of certain asymmetric multilevel grating structures, shown in Fig. 3, enhance the extinction ratio of these devices. Such structures can then enable high-performance nanophotonic devices with cost-effective fabrication on flexible substrates [44,45] for high density displays. The process of fabricating asymmetric multilevel nanostructures is demonstrated in Section 6.

3. Methodology

In this section, a general outline of the processes used in the fabrication of multilevel nanostructures is discussed in the context of fabricating SAMTs. The primary advantage of nanoimprinting using SAMTs compared to 193i nm lithography, is the patterning of precisely aligned multilevel features without the need for nanoscale overlay, in one patterning step. The general methodology for fabrication of SAMTs relies on a combination of nanoscale lithography, atomic layer deposition's (ALD) atomic precision, and highly etch selective material choices, to ensure precise self-alignment of multiple levels in the nanoscale

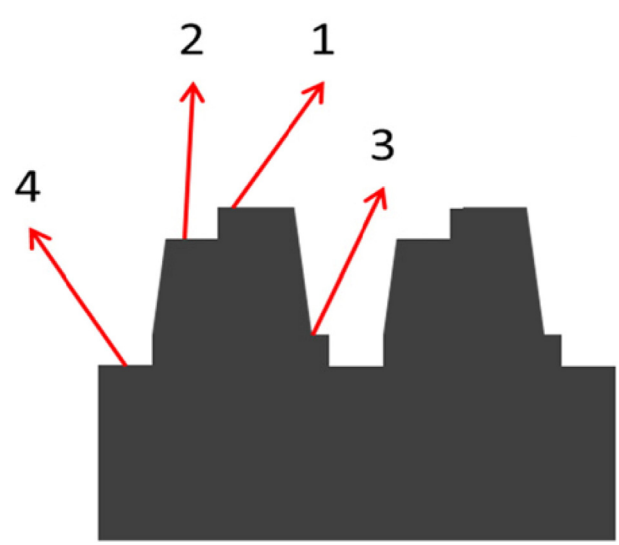

Fig. 3. Illustration of a cross section of asymmetric multilevel grating structures for fabrication of high performance metamaterial wire-grid polarizers.

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