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Research paper

MEMS-based fabrication of high-performance inductors with back hollow structure and ferromagnetic film

Gang Wang [a,b], Houfang Liu [a,b,*], Haochuan Qiu [a,b], Keyu Ning [a,b], Yi Yang [a,b], Xiaoli Li [c], Xiaohong Xu [c], Marion Lavanant-Jambert [d], Sébastien Petit-Watelot [d], Yuan Lu [d], Tian-Ling Ren [a,b,*]

[a] Institute of Microelectronics, Tsinghua University, Beijing 100084, China
[b] Tsinghua National Laboratory for Information Science and Technology (TNList), Tsinghua University, Beijing 100084, China
[c] School of Chemistry and Materials Science, Shaanxi Normal University, Linfen 041004, China
[d] Institut Jean Lamour, UMR 7198, CNRS-Université de Lorraine, BP 70239, 54506 Vandœuvre, France

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A B S T R A C T

The development of novel on-chip device techniques is attracting more and more interest because of the increasing demand for communication electronics, wearable devices and Internet of Things (IoT) with features of low power consumption, high frequency-response, small size, fast transmission rate, and low-costs in the lab-on-chip field. This letter presents the high frequency performance enhancement of on-chip inductors by the use of a back hollow structure filled with CoFeB/ZnO/CoFeB thin ferromagnetic layers. The magnetization dynamic response of this ferromagnetic stacks deposited by RF-magnetron sputtering were investigated. The inductance increases by 41.2%–70.6% between 0.1 and 8 GHz reaching 70.6% at 6.9 GHz. *Q*-factor increases also in a range of 3% to 18% between 0.1 and 3.8 GHz and reach 18% at 1.5 GHz. The equivalent circuit model and simplified physical model of the individual inductor were established and used to model and describe the parameters of inductor, such as the inductance and *Q*-factor as function of frequency. The results show the potential for application of the back hollow structure inductors with ferromagnetic thin film in RF circuits.

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1. Introduction

With recent advances in communication electronics, wearable devices and Internet of Things (IoT), on-chip inductors now require higher *Q*-factors, L-inductance, and frequency response and smaller size, similar to other important RF components, such as voltage-controlled oscillators (VCO) and power amplifiers [1–3]. With the rapid development of science and technology in RF circuits, many efforts have been focused on the on-chip miniaturized inductors with high *Q*-factor and working at high frequency on a standard silicon substrate. Integration of magnetic material into on-chip inductors is one of the most investigated approaches to increase inductance density, quality factor *Q* and/or reduce capacitance and chip area [4,5]. The main requirement for the magnetic film material is to have a high electrical resistivity and a high ferromagnetic resonance (FMR) frequency in order to provide a high-*Q* inductor in the GHz range. Several soft ferromagnetic materials have been used to fabricate on-chip inductors, such as NiZn [6], NiFe [7], MnZn [8,9], CoNbZr [10], CoZrTa [11,12], FeTaN [13], FeNi-SiO_2 [14] and $Y_3Fe_5O_{12}$ [15]. However, low *Q*-factor and poor high frequency response limits their high-frequency application, due to low resonance frequency and eddy current losses. Besides the magnetic materials mentioned above, previous researches on the geometry of the inductors have also been implemented into on-chip inductors aiming for GHz application, such as V-groove inductors with nano-composite magnetic thin films [16,17], suspended MEMS spiral inductors, air-core structure and 3D stacked-spiral RF inductors.

Here, we report a novel structure of on-chip inductor with back hollow structure partially filled with a CoFeB/ZnO/CoFeB ferromagnetic thin film by deep silicon etching process on the back of silicon substrate and RF-magnetron sputtering. The inductance *L* and *Q*-factor of the novel on-chip inductors at high frequency, up to 3.8 GHz, are improved. By using vibrating sample magnetometry (VSM) and FMR measurements, the magnetic and frequency response properties of the CoFeB/ZnO/CoFeB thin film are investigated. The equivalent circuit model parameters are also proposed to analyze and verify the performance of the magnetic on-chip spiral inductor.

2. Experimental methods

An optical microscope photography of the on-chip spiral inductor and 3D-microphotograph of the back hollow structure on the backside of the inductor are shown in Fig. 1. The generating alternating magnetic field induces substrate eddy current, especially at the center of the

* Corresponding authors at: Institute of Microelectronics, Tsinghua University, Beijing 100084, China.
E-mail addresses: RenTL@tsinghua.edu.cn, hfliu@tsinghua.edu.cn (T.-L. Ren).

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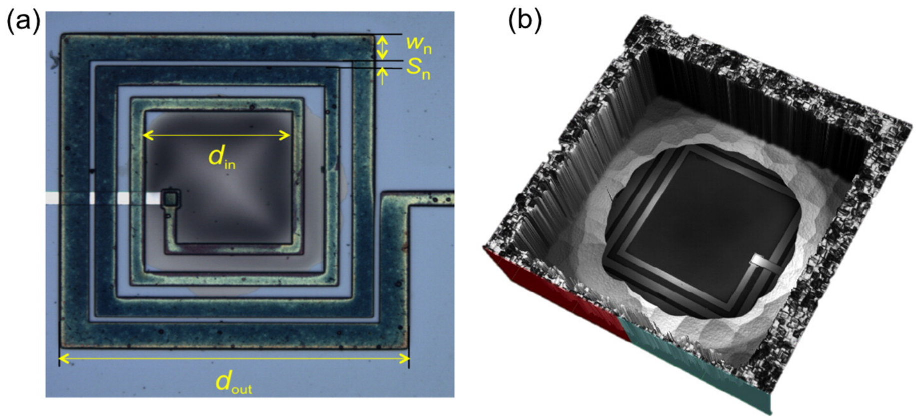

Fig. 1. (a) The optical microscope photography of the inductor. (b) 3D micrograph of the back hollow structure on the backside of the inductor.

inductor coils. So it is effectual that to etch the silicon substrate underneath the inductor coils can decrease the substrate losses.

Using deep silicon etching process and RF-magnetron sputtering, an integrated fabrication process for the on-chip inductor was designed and is summarized in Fig. 2. The CoFeB(100 nm)/ZnO(5 nm)/CoFeB(100 nm) magnetic thin film was deposited by RF-magnetron sputtering technique. The detailed processes flow sketched in Fig. 2 are as follows:

a) A layer of SiO_2 with thickness of 500 nm was deposited on the Si(100) substrate with high resistivity ($\rho > 5000\ \Omega * \mathrm{cm}$) by thermal oxidation process;
b) The bottom electrode of Ti(50 nm)/Pt(150 nm) was deposited on SiO_2 layer by electron beam evaporation process;
c) In order to isolate the bottom and top electrodes, another layer of SiO_2 with thickness of 1.5 μm was deposited on the bottom electrodes by plasma-enhanced chemical vapor deposition (PECVD) process;
d) Via patterns were formed by reactive ion etching (RIE) process;
e) A layer of Ti(50 nm)/Cu(50 nm), which were used as the barrier layer and the seed layer, was deposited by the RF-magnetron sputtering process;
f) The spiral Cu coils with the thickness of 3 μm was fabricated by Cu electroplating process;
g) The barrier layer and the seed layer Ti(50 nm)/Cu(50 nm) were etched by plasma etching process;
h) 3-μm-Thick SiO_2 was deposited on the back of the sample by plasma-enhanced chemical vapor deposition (PECVD) process, which was used as the barrier layer when etched the 500-μm-thick Si;
i) The SiO_2 layer of the region just underneath the inductor coils was etched by reactive ion etching (RIE) process;
j) The 500-μm-thick Si in those regions was etched by back silicon etching process to achieve the back hollow structure;
k) A layer of CoFeB(100 nm)/ZnO(5 nm)/CoFeB(100 nm) thin film was deposited by RF-magnetron sputtering process.

3. Results and discussion

The geometric parameters of the fabricated inductor include number of turns ($n = 3.5$), outer opening diameter ($d_{out} = 500\ \mu m$), width of the inductor coil (w_n), inductor inter-turn space (s_n), with $w_n + s_n = 50\ \mu m$, thickness of the ferrite thin film ($t_m = 200$ nm) and thickness of the Cu coils ($t_{Cu} = 3\ \mu m$). In this structure, the narrower inner metal coils decrease eddy current losses while wider metal coils in the outer turns decrease metal ohmic losses.

The 200 nm-thick CoFeB thin films inserted with 5 nm-thick ZnO layer were chosen as the soft magnetic alloy to increase the resistivity and decrease the eddy current loss. The preparation process of the CoFeB/ZnO/CoFeB magnetic thin film is fully compatible with standard complementary metal-oxide semiconductor (CMOS) processing and

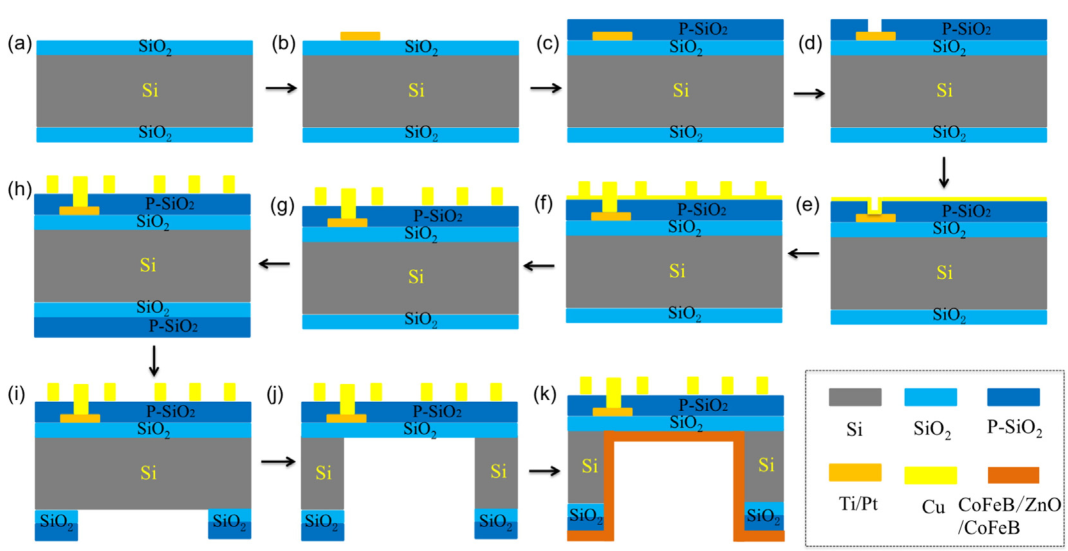

Fig. 2. (a)–(k) The schematic fabrication process of the on-chip inductors with back hollow structure and ferromagnetic CoFeB(100 nm)/ZnO(5 nm)/CoFeB(100 nm) thin film.

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