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Analysis and modeling of the semi-floating transistor based 1T pixel in CMOS image sensors

Jing Gao[a,b,*], Yi Li[a], Zhiyuan Gao[a], Zaifeng Shi[a,b]

[a] School of Microelectronics, Tianjin University, 92 Weijin Road, Nankai District, Tianjin 300072, China
[b] Tianjin Key Laboratory of Imaging and Sensing Microelectronic Technology, 92 Weijin Road, Nankai District, Tianjin 300072, China

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ABSTRACT

A semi-floating gate transistor (SFGT) based 1 T pixel can achieve the same functions as the traditional 3 T active pixel sensor (APS). The SFGT APS improves the fill factor and the pixel density of CMOS image sensors to meet the requirement for high sensitivity application. This paper proposes an equivalent circuit model for the SFGT APS. The model shows that the intrinsic capacitances and the applied voltages affect the SFG voltage range, the maximum non-saturated light power, the conversion gain and the full well capacity (FWC). The simulation results are obtained by technology computer aided design (TCAD), which shows a good agreement with theoretical calculation. A higher drain voltage improves the output swing, the maximum non-saturated light power, the conversion gain and the FWC. A lower capacitance C_{PIP} increases the output level and the conversion gain at the expense of the light range and the FWC. The model also proposes optimization for better pixel design.

1. Introduction

Frohman Bentchkowsky proposed the first floating gate MOS (FG-MOS) to achieve a fully decoded 2048-bit electrically programmable read-only memory in 1971 [1], the floating gate devices had a rapid development over the past few decades [2–6]. The semi-floating gate transistor (SFGT), which embeds a tunneling field effect transistor (TFET) into FG-MOS, has been developed in recent years [7]. The improved structure has many advantages including higher read and write speed, lower operating voltage and smaller chip area [8,9], which can be applied in static random access memory (SRAM), dynamic random access memory (DRAM) [10], ultra low voltage (ULV) logic [11], gamma-ray dosimeter [12] and CMOS image sensor (CIS) [13]. It is difficult to meet the requirement of high sensitivity in the traditional 3 T or 4T APS because of the limited fill factor. An effective method for improving the fill factor is to share one readout circuit by multiple photodiodes to make the average transistor count 1.75 T or 1.5 T in each pixel. But it makes the operation timing and the layout complex. The 1 T pixel could have higher fill factor and higher pixel density with simple pixel structure and operation timing, which performs all the functions as the 3 T APS. And it has advantages of small size and low cost compared with the current image sensors. As the process of SFGT develops, the 1 T APS has a promising prospect in imaging.

This paper analyzes the SFGT device physical characteristics, and establishes a model for SFGT APS. A simulation structure is also built with TCAD. The simulated parameters and operating functions are compared with quantitative calculation. The comparison shows that this model can describe the SFGT APS effectively. The model predicts that the applied voltage and the internal capacitance will affect the device characteristics, which are useful for better pixel design.

This paper is organized as follows. Section 2 presents the architecture and the principle of SFGT APS. In Section 3, the equivalent circuit model and theoretical analysis are detailed. Section 4 shows the calculated and simulated results of the SFGT APS. The factors related with device characteristics are discussed in Section 5. Finally, the conclusion is presented in Section 6.

2. Basic structure and operating principle

2.1. SFGT APS architecture

The equivalent schematic diagram of a SFGT APS is shown in Fig. 1(a). A SFGT pixel unit consists of a photodiode, a NMOSFET and a control gate (CG). The corresponding cross sectional view and the plan view are shown in Fig. 1(b) and (c) respectively. The photodiode located at right side is formed by the shallow P+ layer and the N well, where the shallow P+ layer is directly contacted with the SFG through contacting region and the N well is connected with the N+ doped drain of NMOSFET. The semi-floating gate (SFG) located at left side acts as the gate of NMOSFET. The dielectric material Si_3N_4 isolates the P+

* Corresponding author at: School of Microelectronics, Tianjin University, 92 Weijin Road, Nankai District, Tianjin 300072, China.
E-mail address: gaojing@tju.edu.cn (J. Gao).

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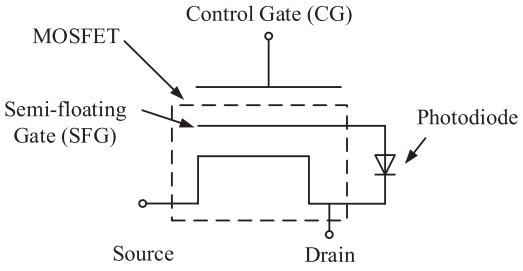
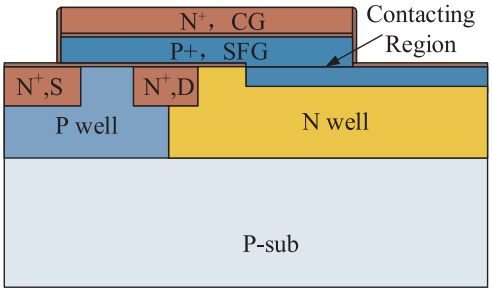
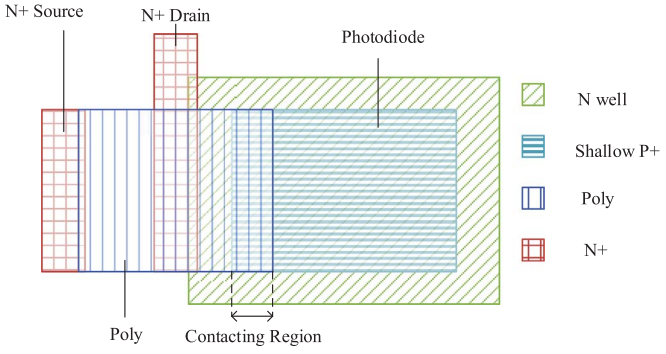


(a) The equivalent schematic diagram of the SFGT APS.



(b) Cross sectional view of the SFGT APS.



(c) Plan view of the SFGT APS.

Fig. 1. The architecture of the SFGT APS.

doped polysilicon SFG from the N+ doped polysilicon CG. A pixel unit consists of four electrodes, which are CG (V_{CG}), source (V_S), drain (V_D) and substrate (V_{SUB}) electrode. In the SFGT 1 T pixel, the drain electrode is connected to the column bus, so that drain current is read out as output signal. The CG electrode acts as a switch for row selection.

2.2. Basic operating principle

One operation cycle consists of four phases, which are a reset phase, an exposure phase, and two readout phases. During the whole process only the CG voltage and the drain voltage change. The source and substrate electrode are always connected to ground. The operation of the two electrodes is shown in Table 1. First, V_{CG} and V_D are set to 3 V and 0 V, respectively, in reset phase. The PN junction photodiode formed by shallow P+ layer and N well operates in forward-biased state, where the discharging current resets the SFG and shallow P+ layer voltage. The drain current drops rapidly and has no effect on the output signal although the pixel is selected. Next, V_{CG} is held at 3 V and V_D rises to 3.3 V, the SFGT APS enters into the first readout phase. The SFG voltage rises to a certain value due to the increased drain voltage. Then the drain current is read out as the first signal of the double sampling. After the first readout, V_{CG} is set to 0 V and V_D is held at 3.3 V, and the exposure phase starts. The SFG voltage drops with V_{CG} due to the capacitive coupling effect. During exposure, the photo generated holes are collected by the SFG under reserve biased electronic field and the SFG voltage continues to increase. Light power and exposure time determine the voltage increase of the SFG. Finally, V_{CG} and V_D are set to 3 V and 3.3 V respectively. The drain current is read out as the second signal of the double sampling. The first readout signal is the drain current where the SFG is reset, and the second signal is that where photo generated charges are collected by the SFG. The difference of the double sampled values reflects the illumination level with reduced reset offset and noise.

Table 1
Operating flow for the 1 T APS.

	Reset	Readout	Exposure	Readout
V_{CG}	3 V	3 V	0 V	3 V
V_D	0 V	3.3 V	3.3 V	3.3 V

3. Device characteristics analysis

3.1. Basic model description

An equivalent circuit model of SFGT APS is established for performance characteristics analysis, as shown in Fig. 2. The poly-insulator-poly (PIP) capacitance is named C_{PIP}, which is formed by dual polysilicon gate and dielectric material Si_3N_4. The PNP structure located at the right side contains two PN junction diodes, which are named PD1 and PN1, and their corresponding capacitances are named C_{PD} and C_{PN} respectively. The substrate and source electrodes are always connected to ground. The capacitance C_{GB} between SFG and ground includes two parts, which are the capacitance C_{GS} between SFG and source, and the capacitance C_{GB0} between SFG and substrate. The overlap capacitance between the SFG and the drain area is named C_{GD}. The drain current of the internal NMOSFET is named I_D, which is determined by SFG voltage during the readout phase.

3.2. Operation analysis

The equivalent circuit model is shown in Fig. 2. In each phase, some components are negligible. Fig. 3 shows the equivalent circuit models at the reset phase, readout phase, and exposure phase. These models are described detailed according to the four operating phases.

3.2.1. Reset phase

In reset phase, the CG and drain are set to a certain high voltage (3 V for example) and 0 V respectively. Since the N well is connected to the NMOSFET's drain, the PD1 operates in forward biased state, and then a discharge current generates on C_{PD}. The SFG voltage drops to the drain

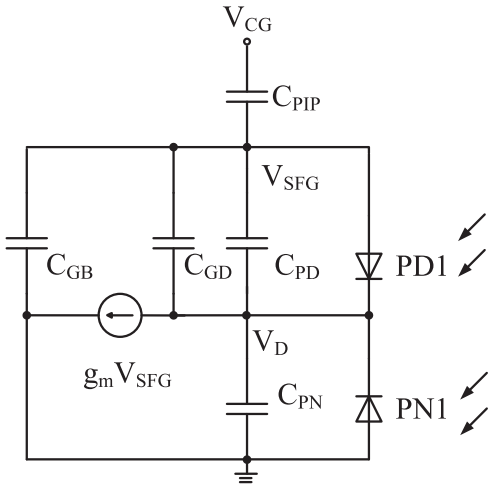


Fig. 2. The equivalent circuit model of the SFGT APS.