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Exploring the short channel characteristics and performance analysis of DMDG SON MOSFET

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ABSTRACT

A two-dimensional (2-D) analytical model for dual-material double gate (DMDG) Silicon-on-Nothing (SON) MOSFETs is developed to study the effect of variation of both the surface potential and threshold voltage on short channel effects (SCEs). Two dimensional (2-D) Poisson's equation with proper boundary conditions has been solved considering the parabolic potential approximation. The model includes the calculations of threshold voltage, electric field and subthreshold swing. The impact of variation of the device parameters such as gate length ratios, gate metal work functions on the performance of the device has been examined and the results are compared to that of dual-material double gate (DMDG) Silicon-on-Insulator (SOI) MOSFETs. The calculated results obtained have been validated with the numerical simulation data obtained from ATLAS, a 2-D device simulator from SILVACO.

1. Introduction

With the advancement of technology in the field of electronic device, an increasing demand for faster device has led to the continuous downscaling of MOSFETs for VLSI applications [1]. However, shrinking the channel length to nanometer range in MOSFETs has significantly degraded the device performances as the threshold voltage gets reduced. This happens due to a decreased control of gate over the depletion region and also due to an increase in charge sharing from source or drain [2]. This effect is popularly known as the Short channel effect (SCE) [3]. Hence, to reduce the various SCEs namely Drain-induced barrier lowering (DIBL), subthreshold characteristics degradation, etc. [4], new structures such as Silicon-on- Insulator (SOI) [5,6] has presently been the topic of high interest to the researchers. Though the high electric fields in MOSFETs have been successfully implemented to achieve high light modulation speed [7] but at the same time, high electric fields can result into Hot Carrier Effects that can increase leakage currents. It is proven fact that SOI is immune to various SCEs, however it suffers from the major drawbacks of threshold voltage roll-off and subthreshold slope reduction [8,9]. In order to get devices with upgraded performance, improved SOI structures have been suggested [10]. Though detailed quantum analysis has been studied on the MOSFET structures but implementation of new technologies like SOI can further improve the efficiency of the device [11]. Better results [12] were obtained when the BOX layer in SOI was replaced by the unity value dielectric, i.e air. This technology popularly known as Silicon-on-Nothing (SON) has reduced parasitic capacitances between source/drain and hence comes with a higher circuit speed [13].

The dual gate (DG) MOSFET has been an interesting topic to the researchers nowadays. With the attractive features like improved transconductance and switching capability, the DG MOSFETs are considered to be quite advantageous over single gate structures when scaled down to sub-50 nm range for VLSI applications. However, using the DG MOSFET alone could not improve the device performance as it suffers from HCEs and subthreshold characteristics degradation when scaled down to nanometer range [2].

To overcome these difficulties multi-material gate engineering [14] has been developed. In this technology, the gate electrode consists of more than one metal-like material having different work functions [15]. Nowadays, dual-material double gate (DMDG) structures are quite popular, with metals or metal-like materials placed in a symmetric manner [16] or the gate electrode being a binary metal alloy (A_xB_{1-x}) having linearly graded work functions [8]. The material with higher work function is placed at the source side to get improved results.

This paper uses the concept of DMDG MOSFET coupled with the SON technology and proposes a model of DMDG SON MOSFET. A comparative study has been carried out between DMDG SOI MOSFET and the proposed DMDG SON MOSFET model to examine the latter's flexibility on SCEs. Device performance variation is observed by varying the gate lengths under the two different metals and the results

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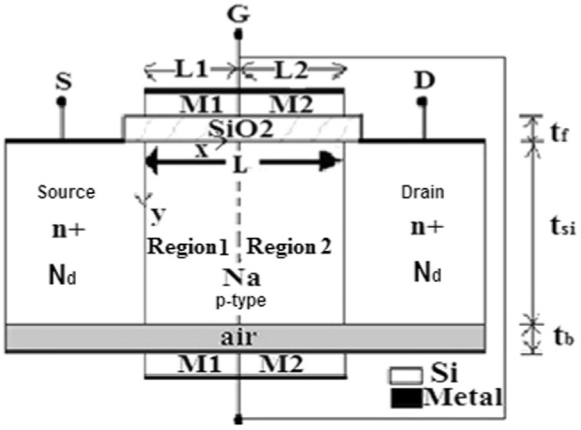

Fig. 1. 2-D Cross-sectional view of the Proposed DMDG SON MOSFET.

obtained are in good agreement with the results obtained using ATLAS 2-D device simulator.

2. Proposed structure and analytical modeling

Fig. 1 shows the 2-D cross-section of the proposed model of DMDG SON MOSFET. The front gate consists of two metals M1(work function $\phi M1$) of length L1 and metal M2 (work function $\phi M2$) of length L2($\phi M1 > \phi M2$). The back gate also consists of M1 and M2. The front and the back gate are kept at same potential Vgs. The channel length is L = L1 + L2, the front oxide thickness is t_f, the silicon film thickness is t_{Si} and the back air thickness is t_b. The channel doping N_a is 1×10^{15} cm^{-3} and that of source and drain denoted as N_d is 5×10^{21} cm^{-3}. The parameters used for calculation and simulation are given in Table 1. In a short channel device, potential distribution in the channel being purely two-dimensional in nature [17], solution of two-dimensional Poisson's equation in the channel region is done to calculate the potential profile of the device. Potential distribution for interpreting the light emission enhancement in Si MOSFETs has already been successfully simulated before [18], in this paper, we opted for an analytical approach and then used the simulated data for validating the analytical results.

2.1. Surface potential modeling

We assume that the channel is fully depleted under zero bias, we also assume that the impurity density and the influence of the charge carriers on the electrostatics of the channel are uniform. Hence the 2-D potential distribution before the onset of strong inversion in the Si channel is obtained by solving the 2-D Poisson's equation [15],

$$\frac{\partial^2 \phi 1(x,y)}{\partial x^2} + \frac{\partial^2 \phi 1(x,y)}{\partial y^2} = \frac{qNa}{\varepsilon si} \tag{1}$$

for ($0 \le \times \le$ L1, $0 \le y \le$ tsi)

$$\frac{\partial^2 \phi 2(x,y)}{\partial x^2} + \frac{\partial^2 \phi 2(x,y)}{\partial y^2} = \frac{qNa}{\varepsilon si} \tag{2}$$

for (L1 $\le \times \le$ L, $0 \le y \le$ tsi)where ϕ1(x,y) and ϕ2(x,y) are the potential distribution functions under M1 in region1 and M2 in region 2 respectively, Na is the uniform doping concentration in the channel, εsi is the permittivity of Si and q is the electronic charge. Considering a parabolic potential approximation [9] in the channel, we can write

$$\phi 1(x,y) = \phi s1(x) + C11(x)y + C12(x)y^2 \tag{3}$$

(under M1)

$$\phi 2(x,y) = \phi s2(x) + C21(x)y + C22(x)y^2 \tag{4}$$

(under M2)

Here, $\phi 1(x,y)|_{y=0} = \phi s1(x)$

Hence, $\phi s1(x)$ is the surface potential below the front gate metal M1 at the SiO_2/Si interface in region 1 under L1 and similarly $\phi s2(x)$ is the surface potential below the front gate metal M2 in region 2 under L2. In order to solve the 2-D Poisson's equation we need to consider the following boundary conditions [19] which are:

i. The tangential electric fields should be continuous at the front gate-oxide interface as well as back gate-air interface.
In Region 1 at the front gate-oxide interface,

$$\left.\frac{\partial \phi 1(x,y)}{\partial y}\right|_{y=0} = \frac{\varepsilon ox}{\varepsilon Si.\ tf}(\phi 1(x,0) - Vgs + Vfb1) \tag{5}$$

In Region 2 at the front gate-oxide interface,

$$\left.\frac{\partial \phi 2(x,y)}{\partial y}\right|_{y=0} = \frac{\varepsilon ox}{\varepsilon Si.\ tf}(\phi 2(x,0) - Vgs + Vfb1) \tag{6}$$

In Region 1 at the back gate-oxide and back channel interface,

$$\left.\frac{\partial \phi 1(x,y)}{\partial y}\right|_{y=t_{Si}} = \frac{\varepsilon air}{\varepsilon Si.\ tb}(Vgs - Vfb1 - \phi 1(x,tsi)) \tag{7}$$

In Region 2 at the back gate-oxide and back channel interface,

$$\left.\frac{\partial \phi 2(x,y)}{\partial y}\right|_{y=t_{Si}} = \frac{\varepsilon air}{\varepsilon Si.\ tb}(Vgs - Vfb2 - \phi 2(x,tsi)) \tag{8}$$

where ε_{ox} and ε_{air} are respectively the permittivities of SiO_2 and air, Vgs is the gate-to-source voltage, Vfb1 is the flat band voltage at the interfaces of region 1,

$$V_{fb1} = \phi M1 - \phi Si \tag{9}$$

Vfb2 is the flat band voltage at the interfaces of region 2

$$V_{fb2} = \phi M2 - \phi Si \tag{10}$$

where ϕSi is the work function of the uniformly doped Si channel,

$$\phi Si = \frac{\chi_{Si}}{q} + \frac{E_g}{2q} + \phi_F \tag{11}$$

where χ_{Si} is the electron affinity of Si and Eg is the band gap of Si in eV. ϕ_F is the Fermi potential of Si, hence for p-type substrate

$$\phi_F = V_t \ln\left(\frac{N_a}{n_i}\right) \tag{12}$$

Where V_t is the thermal voltage and n_i is the intrinsic carrier concentration.

ii. Potential at the source end is

$$\phi 1(0,0) = \phi s1(0) = V_{bi} \tag{13}$$

V_{bi} is the built-in potential in the channel.

iii. Potential at the drain end is

$$\phi 2(L,0) = \phi s2(L) = V_{bi} + V_{ds} \tag{14}$$

Table 1
Typical parameter values used for calculation and simulation of DMDG SON and DMDG SOI MOSFET.

ϕ_{M1} (eV)	ϕ_{M2} (eV)	t_f (nm)	t_{Si} (nm)	t_b (nm)	Channel doping N_a cm^{-3}	Source/drain doping N_d cm^{-3}
4.8	4.6	2	5	2	1×10^{15}	5×10^{21}