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InP DHBT technology for power amplifiers at mm-wave frequencies

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ABSTRACT

An InP Double Heterojunction Bipolar Transistor (DHBT) technology is presented for millimeter-wave power amplifiers at E-band and higher frequencies. Single- and multi-finger transistors with 0.7 μm emitter width and emitter lengths of 5, 7, 10 μm are designed for high frequency and high power applications. The static and AC performances of the fabricated devices are discussed. Reported cutoff frequency and maximum oscillation frequency are f_t = 267 GHz and f_{max} = 450 GHz for a 0.7 × 5 μm^{P2} single-finger device, respectively. Results from large-signal measurements at 30 GHz are reported for single and 4-finger devices. Ballasted devices are introduced to improve thermal behaviour and to increase the limits of the safe operating area (SOA). The SOA is improved approximately by 75% for 4-finger devices with 0.7 × 10 μm^2 emitter. A fabricated monolithic microwave integrated circuit (MMIC) at E-band based on stacked InP DHBTs is presented and its performances reported to demonstrate the power capabilities of the technology.

1. Introduction

Future high-speed wireless communication is likely to take place at E-band and higher millimeter-wave frequencies. For these applications, power amplifiers (PA) with large output powers are needed to extend the transmission distance of the wireless communication link. Given the ever growing demand for wide bandwidths and the continuous down-scaling of devices, it becomes more and more difficult to obtain decent level of power at the transmitter end. InP DHBT technology has emerged as a very promising choice for high-frequency applications and have demonstrated capability to operate in the sub-terahertz domain [1–3] (in [1] a DHBT with 130 nm wide emitter is presented with f_{max} > 1 THz and BV_{ce0} = 3.5 V, in [2] GaAsSb is used as the base material for a DHBT that presents f_{max} > 700 GHz and in [3] f_{max} is as high as 470 GHz while still showing BV_{ce0} = 12 V). Although PA designs in the same frequency range have been proposed based on competing technologies such as GaN HEMTs and SiGe BiCMOS, InP DHBTs exhibit excellent power handling capability as a good compromise between high output power and frequency of operation. PA designs based on InP HEMTs have already been realized obtaining 427 mW of output power with PAE of 19% at 94 GHz [4]. Advancements in technology process allowed GaN based MMICs to be demonstrated operating at E-Band with 1.3 W of output power and PAE of 27% [5] and in the W-band with 3W/mm of output power and PAE of 27.8% [6]. Thanks to more mature technology process and corresponding reliability InP based HBTs remain however interesting for commercial products targeting E-band and higher frequencies. PA designs based on SiGe technology showed an output power of 22-dBm and PAE of 3.6% at 120 GHz [7]. Although the high operating frequency, SiGe technology provides lower output power density levels compared to InP based technology. For all of the mentioned reasons InP DHBT technology is a good candidate to build PA for E-band and higher frequencies and several designs have already been demonstrated up to 0.67 THz [8,9].

Table 1 presents a summary of the state-of-the art transistor technologies for sub-THz applications. The summary includes vertical and planar single-finger devices based on InP, SiGe and GaN and presents relevant performance metrics for PA as cutoff frequency f_t, f_{max} and BV_{ce0}. Although the device technology presented in this work has lower frequency performances than the most recent published results of deeply scaled InP DHBTs, it is important to evaluate these same performances with comparable emitter dimensions in order to assess the advantages and drawbacks of different epitaxial design approaches. The scaling of emitter junction width in InP/InGaAs DHBT is a needed step to reduce charging times and access resistances and capacitances and thus increase device f_{max} [16]. The scaling rule for InP based DHBTs derived in [16] predicts a 2:1 bandwidth increase for a 4:1 decrease in emitter width, assuming that also the vertical dimensions are consequently scaled. Based on this assumption, the InP DHBT design presented in this work show a high potential when compared to other published results as presented in Table 2. It is evident, however, that

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Table 1
Summary of state-of-the-art transistors for sub-THz applications.

Reference	Technology	f_t (GHz)	f_{max} (GHz)	BV_{ce0} (V)
[1] 2011	0.13 × 2 μm² InP DHBT	520	1100	3.5
[10] 2013	20 nm GaN HEMT	454	444	10
[11] 2014	130 nm SiGe HBT	300	500	1.6
This work	0.7 × 5 μm² InP DHBT	267	450	7.5

Table 2
Published InP-based DHBTs performances by emitter width.

Reference	Emitter dimensions (μm × μm)	f_t (GHz)	f_{max} (GHz)	BV_{ce0} (V)
[12] 2013	0.8 × 5	400	350	–
This work	0.7 × 5	267	450	7.5
[13] 2001	0.5 × 8	171	425	8
[14] 2015	0.5 × 6	290	320	≈4
[15] 2015	0.18 × 2.7	404	901	4.3

further performance improvement of the devices presented in this work will need an effort toward device scaling to smaller emitter widths.

Starting from the previous generation of InP DHBT fabricated at III-V Lab for high-speed mixed-signal applications [17], the goal of this work is to adapt the existing transistor technology to the design of power amplifiers targeting E-band and higher frequencies. For power amplification (PA) applications, breakdown voltage and safe operating area (SOA) are the most important device characteristics to improve in order to maximize voltage swing of the amplifier. The design approach for the basic PA power cell in this work starts from the choice of the most suitable single-finger device epitaxial structure and geometrical dimensions. For this purpose, single finger DHBTs with different collector layer thickness and emitter length were fabricated and compared in terms of static and frequency performances. Taking into account the measurements' results, a single-finger device is selected with f_{max} above 400 GHz and $BV_{ce0} > 7$ V. The second step in the design of the PA power cell is to combine the selected single-finger devices in a parallel multi-finger structure in order to increase the output power. However, in high-power applications, InP DHBT multi-finger structures suffer from degradation caused by self and mutual heating between the fingers. Multi-finger DHBTs with up to 8 finger were compared to select the number of finger that provides a convenient tradeoff between output power and frequency performances. For the selected number of fingers the impact of inter-finger spacing was investigated in order to limit the mutual heating effects. As a way to improve the thermal properties of the final multi-finger structure selected for the power-cell, ballasted resistors were introduced that increase the boundary of device SOA.

2. Device structure and process

The starting point for this work is the 0.7 μm InP DHBT technology developed at III-V Lab for high-speed circuits [17]. It demonstrates cutoff frequencies f_t and f_{max} around 300 GHz and a breakdown voltage of 5 V. In this work, this technology is further modified and improved to design MMICs at E-band for power applications. The device is required to demonstrate higher power gain (higher f_{max}) as well as larger safe operating area (higher breakdown voltage). The cutoff frequency f_t is defined as [18]:

$$\frac{1}{2\pi f_t} = \tau_b + \tau_c + r_E(C_{je} + C_{bc}) + (R_E + R_C)C_{bc} \quad (1)$$

where the extracted τ_b and τ_c are the base and collector transit time respectively, r_E is the dynamic base-emitter resistance divided by the current gain β, C_{bc} is the total base-collector capacitance, C_{je} is the base-emitter junction capacitance, R_E and R_C are the extrinsic emitter and collector resistance, respectively.

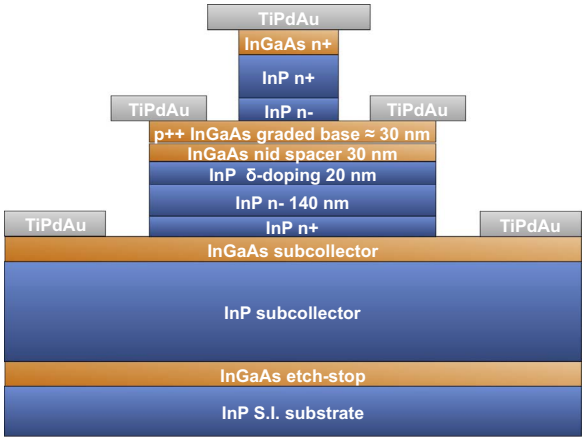

Fig. 1. Schematic cross-section view and simplified layer structure of a single finger DHBT.

According to the approximate expression [18]:

$$f_{max} \approx \sqrt{\frac{f_t}{8\pi(R_{bx}(C_{bcx} + C_{bci}) + R_{bi}(C_{bci}))}} \quad (2)$$

f_{max} is optimized by reducing the product of the extrinsic and intrinsic base resistance (R_{bx} and R_{bi}) and base-collector capacitance (C_{bcx} and C_{bci}).

2.1. Vertical structure

The epitaxial material is grown by Gas Source Molecular Beam Epitaxy on a 3″ semi-insulating InP substrate. The structure consists of a 40 nm InP emitter, a ≈30 nm highly C-doped and compositionally graded InGaAs base and a composite collector. The collector includes a non-intentionally doped (nid) InGaAs spacer, a highly doped InP region and a low doped InP layer. A low-doped InP layer is used to fully deplete the collector at low bias. A simplified structure description of the device is shown in Fig. 1.

In comparison to the structure reported in [17], the composition and doping of the emitter InGaAs cap layer was modified reducing the emitter resistance by half.

The base layer is very thin to minimize the base transit time. This layer is highly carbon doped (≈ 8×10^{19} cm^{-3}) in order to decrease the base sheet resistance. Thanks to the optimization of the epitaxial growth (carbon incorporation), the base sheet resistance has been reduced from 1150 Ω/□to 800–900 Ω/□. This leads to a reduction in the total base resistance and thus in the increase of f_{max}.

The epitaxy optimization process includes the reduction of device self-heating effects occurring at high dissipated power levels. As the thermal conductivity of InGaAs is considerably lower than InP, the general approach consists in the thinning of InGaAs layers [20]. In particular the InGaAs subcollector layer was thinned down from the initial value of 50 nm to an optimal thickness below 10 nm. This modification reduced the overall device thermal resistance by more than 20% while still retaining the same etch-stop function in the technology process. The thermal resistance values extracted from electrical measurements for the current technologies are reduced to about 3300,2600 and 1900 K/W for single-finger DHBTs with L_e = 5, 7, 10 μm respectively.

With respect to [17], the improvement of the emitter cap layers, the reduction of the base sheet resistance and of the thermal resistance led to an improvement in frequency performance as reported in Table 3.

2.2. Process

The DHBTs with an hexagonal shape [17] are fabricated using a