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An 85%-efficiency reconfigurable multiphase switched capacitor DC-DC converter utilizing frequency, switch size, and interleaving scaling techniques

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ABSTRACT

A high efficiency all-CMOS switched-capacitor DC-DC converter (SC DC-DC) with frequency, switch size and interleaving scaling is proposed in order to achieve high efficiency for wireless sensors and internet of things (IOTs) applications. According to the output load current, decision making unit adjusts the frequency, switch size and number of interleavers to match the required current profile and reach steady state. 4-equally-phased clocks are utilized in the design of the SC DC-DC converter. The converter is implemented in 65 nm CMOS process with a peak efficiency of 85% at 600 μA load current. It can supply output current ranging from 20 μA to 5 mA with efficiency higher than 75%. The converter can be configured into 3 different gain topologies to support nominal output voltages of 1.1 V, 1.65 V and 2.2 V, from a 3.3 V input supply. Total area of the converter is 0.725 mm^2.

1. Introduction

Ever increasing value of energy and necessity of longer battery life have led the researchers to focus their efforts into energy efficient and cost effective systems. Additionally, the wide spread use of wireless sensors and IoT applications require cost effective and energy efficient solutions for affordable products such as mobile phones, tablets, mobile sensors and medical systems that have decent performance. In stand-alone mobile devices, all system is powered through a single battery and all the particular supply voltages that are required for each block is generated with a power management unit. The traditional way of generating these supply voltages is using cheap but inefficient linear dropout regulators (LDO) or using efficient but costly inductor based switching buck regulators. Inductor-based switching regulators use bulky and costly off-chip inductors.

There are some efforts to remove these external bulky inductors with on-chip spiral ones or bondwire inductors [1]. However, on chip inductor-based switching regulators suffer from losses due to higher series inductor resistance [1] and require additional costly fabrication steps such as thick metals or integrating ferrite core inductors on the chip [2]. Recently, switched capacitor (SC) DC-DC converters gained attention from both industry and academia as it can be fully integrated on-chip by eliminating the off-chip inductors. On-chip MOS Capacitors can be used in SC DC-DC converters to achieve low series resistance and high capacitance density, and they do not require any additional fabrication steps. These converters are usually implemented using multi-phase interleavers in order to minimize output-ripple that can cause problems in clocked circuits and generate undesired spurs in transceivers. [3] only uses interleaving and switch-size scaling to minimize the output ripple voltage with minimum possible operating frequency.

Controlling SC converters to achieve the highest possible efficiency is challenging especially if the converter supplies a very wide range of load current values. Many fully integrated SC converters with different controlling schemes have been proposed in several past publications. Reference [2] uses pulse frequency modulation scheme to control the converter by using a high speed comparator that cuts the clock feed if the output voltage is higher than its reference. The drawback to this method is the large output ripple, especially at light output load conditions. Reference [4] uses switch width modulation, where it changes the switches sizes according to the output load voltage and current though a lookup table, but this scheme suffers high switch losses at light loads due to constant frequency. References [5,6,7] use pulse frequency modulation, where the load voltage is regulated by changing the switching frequency relative to the load current. This technique can generate uncontrolled tones on the output voltage that can be an issue in wireless applications.

To surmount the obstacle of supplying a wide range of current with high efficiency, we present a combination of Frequency, Switch, and Interleaver Modulation (PFSIM) techniques in a digitally controlled

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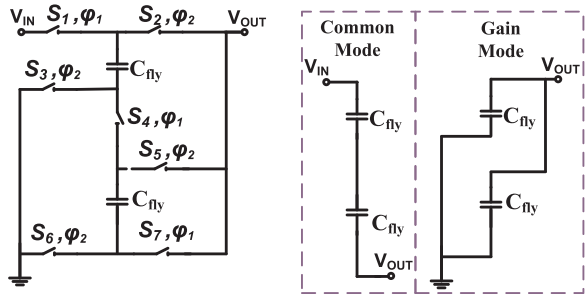

Fig. 1. A 1/3 step-down SC converter and its two phases.

Multi-Gain Step-Down Switched Capacitor DC-DC Converter, and it was designed using high-density on-chip MOS-Capacitors available without extra cost in deep submicron CMOS technologies. The paper is organized as follows: Section 2 introduces SC basics and losses in these converters. Section 3 introduces the detailed implementation of the SC core circuit and the control circuitry. Measurement result of the test chip is given in Section 4.

2. SC DC-DC converter fundamentals

2.1. Basic operation of SC DC-DC converter

The fundamental operation of these converters is explained using the 3:1 step down converter shown in Fig. 1. The switches in the converter operate in two-phases φ_1 and φ_2, and each has 50% duty cycle. Turning the switches on and off in each phase changes the mode of the converter between common mode and gain mode [2]. During the common mode [φ_1], (S_1), (S_4) and (S_7) are on and each of the flying capacitors are charged to $(V_{in} - V_{out})/2$. While in the gain mode [φ_2], switches (S_2), (S_3), (S_5) and (S_6) are on. Each of the flying capacitors are in parallel and directly connected to the output, delivering the charge stored in each capacitor to the load capacitor. Consequently, the output voltage equals to one third of the value of the input voltage source, hence the gain is 1/3.

2.2. Losses of SC DC-DC converters

Switched capacitor converters suffer from various losses that limit their efficiency. The main sources of losses are in the core, as shown in Fig. 2, in the form of intrinsic and conduction losses [$P_{intrinsic}$, P_{Rsw}], losses due to bottom plate capacitance [P_{bp}] and gate drive [P_{Csw}]. Intrinsic and conduction losses can be stem from the output resistance of the converter due to equivalent switched capacitor resistance, R_{SCR}, and on-resistance of the switches, R_{on} [1]. Both of these losses are topology dependent and the sum of these two losses is approximated in (1).

$$P_s = I_L^2 . R_{out} = P_{intrinsic} + P_{Rsw} = \frac{I_L^2}{M_{int} \cdot C_{fly} \cdot f_{sw}} + I_L^2 \frac{R_{on}}{W_{sw}} M_{sw} \quad (1)$$

where M_{int} and M_{sw} are constants based on the converter topology, R_{on} is the switch resistance density, and W_{sw} is the total switch size.

Bottom plate capacitor in a MOS capacitor is formed between the N-well and P-substrate due to the reverse biased junction diode capacitors. These parasitic capacitors are charged and discharged every clock cycle and adds to undesired power loss in the converter. Eq. (2) gives an expression for the loss due to these bottom plate capacitors [1].

$$P_{bott-cap} = M_{bott} \cdot V_o^2 \cdot C_{bott} \cdot f_{sw} \quad (2)$$

M_{bott} is a constant based on the converter topology and V_o is the voltage swing across the bottom-plate capacitor.

Lastly, gate drive loss in the core of the converter is due to the charging and discharging of the gate and layout related parasitic capacitors of the CMOS switches every clock cycle, and can be estimated by (3) below.

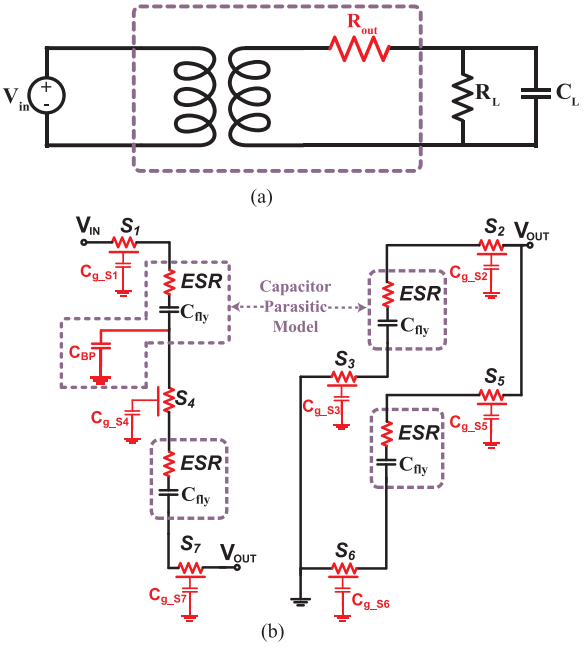

Fig. 2. SC-Core loss sources.

$$P_{gate-cap} = V_{sw}^2 \cdot C_{gate} \cdot f_{sw} \quad (3)$$

where V_{gate} is the total gate capacitance of the switches and V_{sw} is the voltage swing across the switch gates.

In order to generate the multi-phase clocks for interleaving and to achieve tight voltage regulation across a wide range of current loads with high efficiency, a digital control loop is usually employed in these converters. [5,8] This control circuitry and clock generation block tend to use constant power for a given switching frequency during the operation. The power dissipated in these circuitry, [Pctrl], is usually a concern, especially when the output load dissipation is at very low levels. This power dissipation can be divided into switching and leakage losses as in (4).

$$P_{Ctrl} = C_{Ctrl} \cdot V_{IN}^2 \cdot f_{sw} + I_{leak} \cdot V_{IN} \quad (4)$$

where C_{Ctrl} is the equivalent capacitance switched in the clock generation and control circuitry per cycle. I_{leak} is the total leakage current of the circuitry. Taking into account all the above mentioned losses, the power efficiency can be expressed as the ratio between the output power delivered to the load and the sum of all the losses as in (5).

$$\eta = \frac{P_L}{P_L + P_{Csw} + P_{Rsw} + P_{bp} + P_{ctrl}} \quad (5)$$

Among the loss mechanisms discussed above P_{bp}, P_{Csw} and P_{Ctrl} increase linearly with the switching frequency. P_s on the other hand, decreases with the increasing frequency and increases with increasing load current. Consequently, an optimal frequency needs to be chosen for each load current amount for optimal efficiency. Following section discusses the frequency control and other techniques in the design to optimize efficiency across wide range of load currents.

2.3. Output ripple

Size of the output ripples is an important concern in switching regulators since they degrade the performance of the blocks the converters are supplying by introducing spurs. These ripples are mostly due to the charging and discharging of the equivalent output capacitor in