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Adaptive and optimum multiport readout of non-gated crossbar memory arrays

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ABSTRACT

Non-gated crossbar memory arrays are becoming strong candidates to replace the current gated arrays due to their much higher density. Sneak paths are the main problem in gate-less arrays. In this paper, we analyze a three reading multiport readout method for non-gated memory arrays, study its limitation versus the OFF/ON impedance ratio of the memory cell as well as the ratio between the 1 s and 0 s memory cells. We provide an accurate threshold that increases the noise margins that takes these factors into consideration and we also introduce an adaptive threshold that tracks the 1 s and 0 s density variations over time. Finally, we propose a sensing circuit that accumulates the three reading without the need for extra complicated circuitry to evaluate the read memory cell value.

1. Introduction

The International Technology Roadmap of Semiconductors (ITRS) considers future memories based on memristors to be similar or better than existing CMOS-based nonvolatile memories (Flash) [1]. A clear advantage is their scalability owing to the filamentary conduction and switching mechanisms [1]. The two factors which follow scalability in the evaluation criteria of ITRS when assessing future memory technologies are speed and energy efficiency. Among the promising emerging memristive devices are: Conductive Bridging RAM (CBRAM) [2] in which a conductive filament is either formed or dissolved due to redox reactions between two electrochemically-different electrodes placed in an electrolyte, and Oxide-based RAM (OxRAM) [3] which depends on resistance switching of an oxide layer, which may be unipolar or bipolar, due to filament formation or change in tunneling characteristics [1].

Beside memories [4], memristors have many other applications in computing [5], analog circuits as oscillators [6] and modulators [7], and emulating neural networks [8]. Consequently many models were proposed to model memristors for circuit simulation purposes [9–11]. Recently, the memristors were investigated as non-volatile memory cells [4]. The memristor memory array is composed of crossbar structure which is formed of memory cells placed at intersection points between upper and lower bars where the upper bars are placed in the form of columns and the lower bars are placed in the form of rows. To select a memory cell, the corresponding row and column are selected. This structure can be gate-less i.e. it does not need a switch at each cell. Because there are no switches to isolate the memory cells, the density of the whole array increases significantly. The crossbar memory array can be used in Multi-purpose Processing-In-Memory (MPIM) systems [12].

One of the main problems in the gate-less array is the sneak paths [13]. Sneak paths are the undesired paths parallel to the cell intended to be read from or written to. There were some proposed techniques that solve the sneak paths problem [13–15], the simplest and most accurate one is the method presented in [15].

In this work, we correct the threshold used for detecting the information stored at the memory cell by the method introduced in [15] as well as showing the limitations on this threshold. Also, we analyze the effect of the 0/1 distribution in the memory array on the correctness of the readout as well as the method of choice of the threshold to minimize this effect. We also propose an adaptive threshold that can detect the cell value at any 0/1 distribution and is updated either statically or dynamically. Finally, a circuit for performing the three readings without the need to store and then restore the readings is proposed. Our technique is generic enough to be used in crossbar memories with other cells such as memcapacitors.

This paper is organized as follows: the crossbar memory array is discussed in Section 2 where subsection *A* shows the readout method and the threshold used, subsection *B* shows how to choose this threshold to overcome limitations on cell distribution, subsection *C* shows how to make an adaptive threshold according to the 0/1 distribution among cells and finally subsection *D* shows the circuit used for performing the readout. Section 3 shows the simulation results and finally, the paper is concluded in Section 4.

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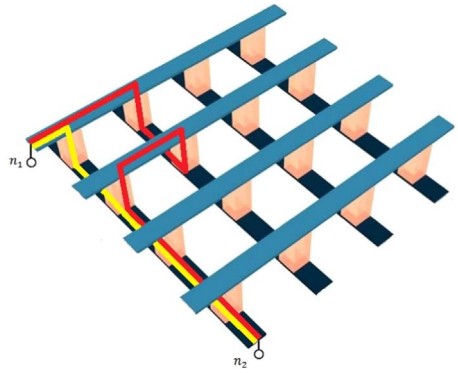

Fig. 1. The main path is in yellow, while the red path is an example of a sneak path.

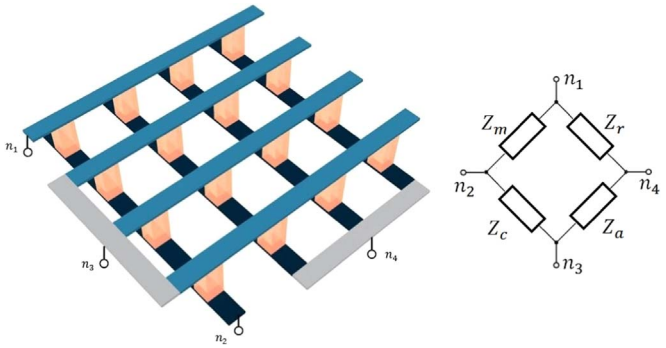

Fig. 2. 3-D crossbar structure using the technique introduced in [14] and the equivalent impedance network on the right.

2. Crossbar memory array

The crossbar structure of the memory array is composed of memory cells placed at intersection points between upper and lower bars where the upper bars are placed in the form of columns and the lower bars are placed in the form of rows. To select a memory cell, the corresponding row and column are selected. A crossbar memory array can be gated or non-gated. The cell in the gated crossbar memory array is associated with a switch to isolate the intended cell from the other cells. In the non-gated crossbar memory arrays, the cells are not isolated with switches; this makes the memory array denser but causes the effect of sneak paths to rise.

The problem of the sneak paths arises because when a certain cell is selected, current does not flow in this cell only but can find other paths between the selected row and column as shown in Fig. 1. This causes a problem when we sense the value of the selected cell to read the stored information as the other paths parallel to the path through the selected cell will affect the reading. The memristive crossbar memory array uses memristors as memory cells at the intersection between bars. Several methods were proposed to solve the sneak paths problem in the memristive memory array [13–18] but the most advantageous method is the one presented in [15]. The method presented in [14] needs three read, three write and one compare operations to be performed. The method proposed in [13] relies on using another memristor as a selection device, instead of the transistor, in series with the information-storing memristor to suppress sneak paths but it does not fully remove their effect. The method in [15] however, fully removes the sneak paths effect by only three reading and one compare operations and it does not use write operations which is an important advantage for the device's endurance.

The more recent methods [16–18] add dumb rows or columns and use less reading operations than [15]. However, these methods depend on some assumptions in order for the method to perform properly unlike [15] which extracts the information mathematically. The methods [16,17] use assumptions such as large array size, large OFF/ON ratio, and sufficient number of ON cells to make the sneak current nearly constant across same-row cells [16], or make it linearly dependent on the number of ON cells in the selected column [17]. The method [18] applies for memristors possessing diode-characteristics in which the reverse resistance is much higher than the OFF resistance in order to assume that the voltage drop on a sneak path is dominated by the voltage on the reverse-biased memristor in that path. However, in [15], a distinction between binary levels always exists and our proposed work in the following subsection defines an appropriate threshold that lies in this distinction.

2.1. Reading process

The method in [15] is shown in Fig. 2. It is important to note that the following analysis is valid if we assume an impedance Z instead of every resistance R as shown in [19]. This substitution allows us to deal with generic memory cells such as memcapacitors in which each R is replaced with $1/C$ as shown in Section 3.

The intended cell is assumed to have a resistance R_m which has one of two possible values: low resistance R_{on} or high resistance R_{off}. The selected column is connected to node n_1, the selected row is connected to node n_2, all the unselected columns are shorted together and connected to node n_3 and all the unselected rows are shorted together and connected to node n_4 as shown in Fig. 2. By doing this, we have four variables: the resistance R_m of the required cell which is between the nodes n_1 and n_2, the resistance R_c of the cells along the column of the selected cell other than the required cell which are between the nodes n_1 and n_4, the resistance R_r of the cells along the row of the selected cell other than the required cell which are between the nodes n_2 and n_3 and the resistance R_a of the cells that are not along neither the row nor the column of the required cell which are between the nodes n_3 and n_4, this is shown in Fig. 2. By performing three readings to sense the resistance between nodes n_1 and n_2 ($R_{1,2}$), n_1 and n_3 ($R_{1,3}$) and n_2 and n_3 ($R_{2,3}$) while n_4 is let floating. According to Fig. 2, the readings are as follows:

$$R_{1,2} = \frac{R_m R_c + R_m R_a + R_m R_r}{R_m + R_c + R_a + R_r},\quad R_{2,3} = \frac{R_m R_c + R_c R_a + R_c R_r}{R_m + R_c + R_a + R_r},$$
$$R_{1,3} = \frac{R_m R_a + R_m R_r + R_c R_a + R_c R_r}{R_m + R_c + R_a + R_r} \tag{1}$$

By eliminating R_c, R_a and R_r, we get the following result [15]:

$$R_{1,2} = R_{2,3} + R_{1,3} + R_m \pm \sqrt{4R_{2,3}R_{1,3} + R_m^2} \tag{2}$$

According to [15], the $'+'$ is selected when $R_m = R_{on}$, and the $'-'$ sign is selected when $R_m = R_{off}$. But since $R_{1,2} < R_m$ because $R_{1,2}$ is composed of R_m parallel to other resistances, we must only take the minus sign of the square root in Eq. (2) as a valid solution.

It has to be noted that $R_{2,3}$ and $R_{1,3}$ are composed of a lot of parallel paths and so, their values are much less than R_m. We use this fact to propose a simplification of the solution given in [15]. So, we can assume that: $4R_{2,3}R_{1,3} \ll R_m^2$. Using Taylor's expansion, we can use the approximation: $\sqrt{4R_{2,3}R_{1,3} + R_m^2} \approx 2R_{2,3}R_{1,3}/R_m + R_m$, so, Eq. (2) reduce to the following expression:

$$R_{1,2} \approx R_{2,3} + R_{1,3} - \frac{2R_{2,3}R_{1,3}}{R_m} \tag{3}$$

We define the variable R_t as follows:

$$R_t = R_{2,3} + R_{1,3} - R_{1,2} = \frac{2R_{2,3}R_{1,3}}{R_m} \tag{4}$$

But since R_m has only two possible values which are R_{on} and R_{off}, and so R_t has two possible expressions: