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CCII and RC fractance based fractional order current integrator

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ABSTRACT

Integrators are an important functional module of several filters, PID controllers and automated systems. Designing these integrators in fractional domain enhance their operations and make the responses highly precise and accurate. This paper presents a Fractional Order Current Integrator using second generation current conveyor as the active block, and fractional capacitor as a grounded fractance. Analog realization of this fractance comprises of resistances and capacitances arranged in parallel RC ladder topology. The motivation behind this work is that more accurate and stable fractional integrator with fewer passive elements, for lower bias voltage and high dynamic range, can be designed and implemented. Integrators of fractional orders from 0.1 to 0.9 are simulated using TSMC 0.25 μm technology parameters. The transient and frequency responses obtained in Mentor Graphics are in close conformity with the theoretical values of magnitude and phase. Robustness of the proposed model is verified by performing Monte Carlo analysis in time and in frequency domain. Comparisons of fractional order current integrators with existing analog fractance models have also been included to further validate the work presented in the paper.

1. Introduction

The modeling of real world physical processes as integer models provides an estimated view of their performance. However, these processes are generally fractional in nature. The ease in designing and on chip availability of integer order systems is the key motivation behind their vast utilization. But nowadays, the feasibility and advancement in implementing fractional order systems has extended its applications in the area of controllers, optics, fluid mechanics, signal processing and biomedical engineering [1].

Fractional order systems exhibit exact responses for wide range of frequencies. For precisely designing such systems, active elements that provide good responses at high frequency are a prime requirement. Second generation current conveyor (CCII) is one such block. It is not bounded by the gain-bandwidth product, as compared to the Op-Amps. CCII was introduced by Sedra and Smith in 1970 [2], as a variant of CCI. CCII is a three terminal unity gain active device with input ports X & Y and output port Z. The ideal equations of the ports of CCII are

$$V_{Xp} = V_{Yp} \tag{1}$$

$$I_{Zp} = \pm I_{Xp} \tag{2}$$

$$I_{Yp} = 0 \tag{3}$$

where, V_{Xp}, V_{Yp} are the voltages at the X & Y port; I_{Xp}, I_{Yp}, I_{Zp} are the currents leaving X, Y & Z ports, respectively. In (2), '+' represents CCII + & '−' CCII −. CCIIs are widely being utilized as building block in advanced circuits of both integer and fractional domain. This is due to the fact that CCII is capable of working in all the three modes: voltage mode, current mode and mixed mode [3,4]. Further, CCII has inherent features of low biasing voltage, ideal port impedances, optimal parasitic impedance level, wide frequency band of operation and expandability [5,6]. In literature, several CCII based integer order applications are designed [7,8].

For realizing systems in fractional domain, a device called fractance or fractional impedance is incorporated. It introduces the fractional behavior in any circuit and is defined as s^{α}; α being positive or negative fractional order and s the complex frequency. This fractance can be realized using analog passive elements [9–27] or electrochemically [1,28,29]. The electrochemical fabrication of two-terminal fractional capacitor is based on the concept of metal-insulation-liquid interface, reported in [1]. The functioning of this fractance is investigated in fractional circuits of [1,28].

Apart from this, the analog equivalent circuits of s^{-m} fractance ($0 < m < 1$) using passive elements based on Newton process of approximation [9] and based on poles and zeros of approximated transfer function [10] are also designed. To design the $s^{-0.5}$ fractance, a solution with constant valued R & C combination is used in domino ladder structure [11] and in tree, H, netgrid and 2-circuit series topology given in [12,13,23]. Arranging passive elements in parallel RC ladder with their consecutive values in G.P., is also a convenient

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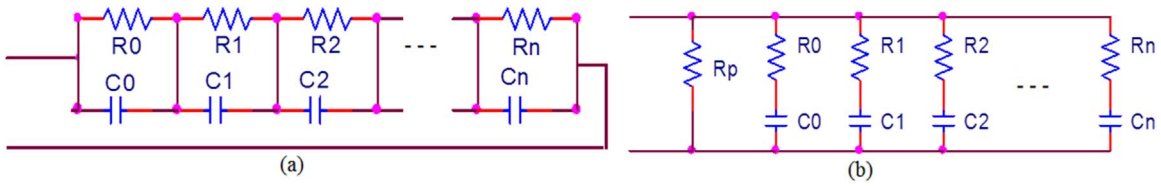

Fig. 1. Fractance design for (a) $-1 < \alpha < 0$ (b) $0 < \alpha < 1$ [10].

structure utilized by researchers to realize passive filters [14], second order passive filters and op-amp based KHN and Salen-Key filters [15].

Considering the properties of CCII and dynamics of fractance, various fractional order filters have been illustrated in literature. In all such circuits, fractional integrators play a significant role. Although, passive realization of integrator provides a simple and cost effective synthesis procedure, but it introduces the loading effect. However, use of active elements reduces this effect considerably.

The major contributions of the paper are:

i) A robust and stable active realization of current mode Fractional Order Current Integrator (FOCI) using CCII+ and passive RC fractance is proposed.
ii) Using the passive RC fractance [25], fractional capacitors of all orders of α, α ϵ(0,1) are simulated. Combining these fractances with current conveyor (CCII), current mode fractional integrators of all orders of α are developed.
iii) As the model of fractance in [25] uses lesser number of passive elements (resistances and capacitances) as compared to several other models presented in literature [10–15,28], the authors have selected this approach for their fractance design. This has made the design simpler.
iv) Grounded RC fractance has been implemented in the paper. This provides two advantages – one that all stray capacitances are eliminated and second that it facilitates IC implementation.

A brief background of various approaches to design α-fractance is included in Section 2. Section 3 presents the CCII based circuit of FOCI. The simulation results of different fractional orders of FOCI, in both time and frequency domain, are compiled in Section 4. Variation in resistances and capacitances of the fractance are introduced and Monte Carlo (MC) analysis is performed. The behavior of the system is evaluated in both time and frequency domain. These simulations also validate the robustness of circuit. A comparison of the effect of different fractance topologies on the output of FOCI is also included in this section. Section 5 concludes the work.

2. Background of α-fractance design methods

Theoretically, the impedance, Z(s), is defined as

$$Z(s) = s^{\alpha}A \tag{4}$$

where, A = Z(s) | denotes the magnitude of Z(s). Depending on the value of α, Z(s) represents different passive elements i.e. for $\alpha = 0$: it is a true resistor, for $\alpha = 1$: true inductor & for $\alpha = -1$: true capacitor. In the ranges $-1 < \alpha < 0$ & $0 < \alpha < 1$, it represents Fractional capacitor (FC) and Fractional inductor (FL) respectively. FL and FC are together termed as α-fractance or fractional impedance, $(\alpha \in R)$.

Analog realization of fractance involves an arrangement of analog elements such as Resistances and Capacitances (R & C) or Resistances and Inductances (R & L). This provides the fractional impedance [30]. The resistance and capacitance combination is preferred, as it is robust and easy to implement because of its high availability.

$$\Phi = (90\alpha)^{\circ} \; or \; (\pi\alpha/2)\text{rad} \tag{5}$$

Eq. (5) gives the relation between α and Φ for α-fractance i.e. phase (Φ) is a function of a fractional order α. For a particular α, the α-fractance exhibits a constant phase (Φ) throughout the operating frequency band; therefore, it is referred to as constant phase element (CPE). Substituting value of α in (5), FC has phase in the range -90° to 0° and FL has phase in range 0° to 90°.

Thus, the synthesis of α-fractance involves a combination of resistances & capacitances as a network s.t for a fixed value of α, the phase remains constant in the desired frequency range of interest. Theoretically, this network should have an infinite structure but for all practical purposes, it is truncated to finite length architecture [11]. The prime objective of this design is to have lesser number of elements, to make it cost effective, simple and feasible to realize on chip. We discuss three different methodologies for designing of α-fractance proposed in literature.

2.1. Rational approximation method

As analog realization of fractional systems cannot be performed directly; their transfer functions are mapped to equivalent approximated integer order transfer functions, using rational approximation methods. Carlson approximation, Charef approximation, Matsuda approximation, Oustaloup approximation and Least Square approximation methods are few of them [31].

The approximated transfer function of s^{α} is expanded into partial fractions to obtain poles (p_i), residues (z_i), and gain (k), where $i = 0, 1, 2 \ldots N$ (N is the total number of poles or residues). In [10] the author has proposed α-fractance formation as: the values of resistances R_i, capacitances C_i and equivalent impedance $Z(s)$, are calculated for $-1 < \alpha < 0$ using (6) and these passive elements are arranged as in Fig. 1a; whereas for $0 < \alpha < 1$, the values of R_i, C_i, R_p and the equivalent admittance $Y(s)$, are calculated using (7) and arranged as in Fig. 1b

$$R_i = z_i,\; C_i = \frac{1}{p_i R_i},\; Z(s) = \sum_{i=0}^{N} \frac{R_i}{1 + sC_iR_i} \tag{6}$$

$$R_i = \frac{1}{p_i C_i},\; C_i = z_i,\; R_p = \frac{1}{k},\; Y(s) = \frac{1}{R_p} + \sum_{i=0}^{N} \frac{sC_i}{1 + sC_iR_i} \tag{7}$$

A major limitation of this method is that it requires large number of passive elements (10–20 each), and the values of capacitances may exceed 1 Farad (1 F) in some cases, which becomes unrealizable.

Iterative methods like Carlson and Matsuda are recursively applied to obtain the approximated rational function. In order to improve the approximation, larger number of iterations of the recursive formulae are performed. However, in doing so, the degree of the resultant polynomial increases, making the system unstable. Hence, there is a trade-off between accuracy of approximation and stability of the system.

2.2. Constant valued passive elements

In this technique the values of the passive elements used are all the same. Different topologies such as H, tree and netgrid for design of α-fractance are elaborated in [12,13]. Fig. 2a, b and c show the equivalent circuits for 0.5-fractance, $Z_{1/2}$, for each topology.

These architectures are recursive, infinite length and symmetric [8]. In Fig. 2, $Z_{1/2}$ is given as