Microelectronics Journal 65 (2017) 49–57

Contents lists available at ScienceDirect

Microelectronics Journal

journal homepage: www.elsevier.com/locate/mejo

Accurate charge transport model for nanoionic memristive devices

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ARTICLE INFO

Keywords:
Memristor
Model
Hybrid circuit
SPICE
Tunneling
Thermionic
Ohmic current

ABSTRACT

Memristors have the potential to significantly impact the memory market, and have demonstrated the potential for analog computing within a sub-class of neuro-inspired information processing. In order to enable circuit designers to use and test memristor/CMOS hybrid circuits, it is necessary to have an accurate and reliable memristor model. In this work, a new memristor model based on Charge Transport Mechanism (CTM) is presented. This paper analyzes different current mechanisms that exist in Schottky barrier region of memristors: direct tunneling, thermionic emission, and Ohmic currents. The proposed memristor model is based on direct tunneling and Ohmic conduction, and it accounts for physical phenomena within memristive devices. The presented model shows a relative root mean square error of about 0.25 when compared with experimental results for a Ag/TiO_2/ITO memristor. It also shows better accuracy in comparison with other modeling approaches published in the literature. The proposed model is implemented in SPICE and a subcircuit for the model is provided.

1. Introduction

The memristor (memory-resistor) was first theorized as the fourth fundamental circuit element by Leon Chua in 1971 [1]. In 2008, Hewlett-Packard laboratories (HP Labs) announced fabrication of a physical memristor device [2]. The resistive switching effects in memristive devices promise an emerging alternative for flash memory, which has limitations in the sub 20 nm range. The Valence Change Memory (VCM) effect is a special type of resistive switching in redox-based devices [3]. VCM memristors offer bipolar switching behavior due to valency change within specific transition oxides like TiO_x, HfO_x, TaO_x and $SrTiO_3$. Following the recent advancements in the memristor-based applications, several models have been developed for implementation in SPICE-like simulators. These models can be the base for designing and simulating future memristive-based analog and digital systems. Due to either the complexity or inaccuracy of previous models, it is necessary to develop an accurate model that can be used in SPICE-like circuit simulators and closely matches experimental data.

In this paper, we present a new physics based memristor model that incorporates ionic transport and tunneling mechanisms. The proposed model is based on data extracted from a fabricated memristor with a Ag/TiO_2/ITO structure [4]. The developed model can be easily utilized as a macro model in SPICE-like circuit simulators such as HSPICE®and SPECTRE®. The noise aspect of charge/trap hopping and effects of process variation within memristor devices are beyond the scope of the presented work.

The paper is organized as follows: Section 2 defines memristor device functionality. The most important models of memristor devices are discussed in Section 3. In Section 4 different memristor charge transport mechanisms are discussed. In Section 5, the proposed model is presented with its SPICE code. The applicability of the model is tested for various input stimuli with different shapes, amplitudes, and frequencies in this section. In Section 6 the behavior of the proposed model is discussed and its accuracy is compared with state of art models. A conclusion of the presented work is provided in Section 7.

2. Memristor device functionality

The memristor is a special class in a more general family of memristive systems and can be either a voltage-controlled or current-

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http://dx.doi.org/10.1016/j.mejo.2017.05.006
Received 24 July 2016; Received in revised form 8 March 2017; Accepted 13 May 2017
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controlled. From this point on, it is assumed that the term memristor refers to the physical memristive device developed for the work in this paper. The behavior of the *N*th order current-controlled memristor is defined through,

$$V_M(t) = M(u, i, t)i(t) \quad (1)$$

$$\dot{u} = f(u, i, t), \quad (2)$$

where u is a vector and it represents N internal state variables. The parameters $V_M(t)$ and $i(t)$ are the voltage and current across the memristor device, respectively and M is called memristance (memory resistance). The charge-controlled ideal memristor is a particular case of Eqs. (1) and (2), where memristance becomes a function of charge,

$$V_M = M(q(t))i, \quad (3)$$

and current is defined by: $i = dq/dt$. The pinched hysteresis loop in the *i-v* characteristic is a unique feature of memristors. It demonstrates the passive nature of these devices as M is always positive. By increasing the excitation frequency, the hysteresis loop shrinks, and it will approach a single line as the input frequency approaches infinity. A schematic illustration and *i-v* curve of Ag/TiO_2/ITO memristor [4] are depicted in Fig. 1. The initial resistance of the device is 172 Ω. The memristor-based circuit for simulation is comprised of a serially connected input voltage source with a Ag/TiO_2/ITO memristor where the positive side of the voltage source is connected to the doped side of the memristor. The common node between the negative side of the voltage source and the undoped terminal of the device is grounded. The input voltage is one period of a 1 Hz triangular wave with a range of −2 V to 2 V.

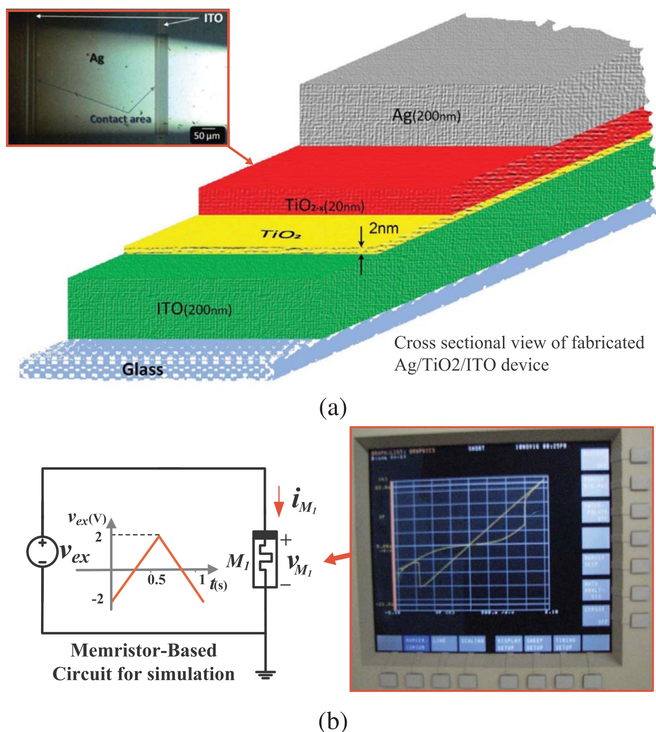

Fig. 1. (a) A cross-sectional view of the Ag/TiO_2/ITO memristor with a fabricated memristor micrograph [4] is illustrated. The Ag and ITO top and bottom electrodes have a 200 nm width each while the thickness of the TiO_2 is about 22 nm. In this case, the doped and un-doped regions have thickness of 20 nm and 2 nm, respectively. The whole structure is placed on top of a glass layer because of the transparent nature of Indium Tin Oxide (ITO) electrodes [4]. (b) The *i-v* characteristic of the physical Ag/TiO_2/ITO memristor device that was obtained using a Keithley 4200-SCS semiconductor parameter analyzer [4]. The proposed circuit and the triangular excitation input voltage are also displayed.

3. Review of memristor models

The first memristor modeling effort [2] considered it to be two resistors in series. In this model, the memristance of device is dependent on the ratio between the thickness of doped region within the dielectric layer and the total dielectric thickness (*D*). The dopants velocity decreases at the edge of the thin film, and this non-linear effect is modeled using a windowing function. A number of efforts to model the non-linearity aspect of these devices using windowing functions have been demonstrated [5–7], however the accuracy of these models is limited. Subsequently in [8], changing modeling approach and using non-linear functions for simulating memristor device behavior have resulted in a non-linear boundary drift model. The non-linear ion drift model of memristors, like the linear ion drift model, is divided into doped and undoped regions that are represented by two separate series resistors. Due to the non-linear dependency between the derivative of the state variable, the thickness of the doped region along insulator film, and voltage, this model is considered non-linear. However, this modeling approach is unable to accurately model the switching behavior of the device.

In [9], a new assumption for memristor modeling considered memristor as a resistor in series with an electron tunnel barrier. The state variable in this model is Simmons tunnel barrier width [28]. This model provides a programming threshold, so change in the state variable is only occurs for current values higher than the threshold current. Due to the impact of the exponential function, there is no need for defining a window function. A SPICE based model that utilizes the Simmons tunnel barrier was proposed in [10]. Although it is complex and has a high computation time, the model is more accurate when compared to the previous models. In [11], the electron tunnel barrier model [9] is modified to avoid non-convergence, numerical errors, and non-physical solutions during time-domain simulation. Also, two physics-based models have been proposed recently for TaO_x-based devices [12,13]. The model in [12] considers TaO_x-based devices with a circuit model that consists of a Schottky barrier diode in low resistance state, a variable resistor, and a base-layer resistor. In [13], modeling is based on incorporating the tunneling probability factor between the metal layers and the semiconductor layer, and demonstrating its effect on the conduction mechanism.

Another popular model is described in [14] that uses a piecewise modeling approach [15] when determining the rate of change in memristance. In [14] the window function is eliminated and another function is implemented to model the tunneling phenomena and asymmetric switching behaviors of the memristor. This causes a high non-linearity in one of the memristance boundaries and a low non-linearity at the opposite side. This model shows a high accuracy and good adaptation of tunneling phenomena like [10].

A more simplified model with lower accuracy, when compared with [16], was presented in [17]. In this model, unlike the other predictive memristor models, the *i-v* relationship can be adapted according to data from every *i-v* characteristic of memristor devices based on setting their related threshold voltage. In addition to its generality in comparison with Simmons tunnel barrier model [9], it uses simpler mathematical functions to achieve the same physical memristive behavior. The effective electric tunnel width is an internal state variable in this model. It has two window functions that limit the internal state variable. This model shows an acceptable accuracy, but it is still lower than that of the Simmons tunneling barrier model.

As an alternative the mentioned predictive models in the literature, [4,18] are applied to measured data and evaluated by fitting an experimentally measured *i-v* curve from a fabricated memristor. The compact model [18] based on experimental observations was developed to account for irregular *i-v* characteristics. In this case a simple compact model that describes the behavior of chalcogenide based memristor devices is presented. Although this model shows better accuracy in comparison with the predictive models, it does not present

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